

Mark M. Tehranipoor

Fellow of IEEE, ACM, AAIA, AIIA, ASEMFL, and NAI

Intel Charles E. Young Preeminence Endowed Chair Professor in Cybersecurity

Sachio Semmoto Chair, Department of Electrical and Computer Engineering, University of Florida

URL: <https://tehranipoor.ece.ufl.edu/>, Email: tehranipoor@ece.ufl.edu

Research Interests

Cyber and Hardware Security, IoT Security, Supply Chain Security, Reliable Circuit Design and Analysis, and Integrated Circuits and Systems Testing

Academic Appointments

06/25-present University of Florida Distinguished Professor
05/22-present Sachio Semmoto Chair, Department of Electrical and Computer Engineering (ECE), University of Florida
06/20-09/21 Co-director, Center for Aerospace Resilience (CAR)
04/20-04/24 Founding Director, Edaptive Computing Inc Transition Center (ECI-TC), URL: <https://ecitc.org/>
07/19-05/22 Program Director of Cybersecurity Program at the University of Florida
07/17-07/19 Associate Chair for Research and Strategic Initiatives (ACR), ECE Department, University of Florida
05/19-04/25 Co-director, AFOSR/AFRL Center of Excellence on Enabling Cyber Defense in Analog and Mixed Signal Domain (CYAN)
05/19-Present Co-director, DOD Microelectronic Security Training (MEST) Center
008/19-08/22 Term Professorship, University of Florida
01/19-present Affiliate Professor and Executive Committee Members, SECURE center, Prairie View A&M University
07/15-Present Intel Charles E. Young Preeminence Endowed Chair Professor in Cybersecurity, University of Florida
07/15-05/22 Director, Florida Institute in Cybersecurity (FICS) Research
URL: <http://fics.institute.ufl.edu/>
11/13-07/15 Professor, University of Connecticut
12/11-07/15 Founding Director, Center for Hardware Assurance, Security and Engineering (CHASE), University of Connecticut
06/12-07/15 Founding Director, Comcast Center of Excellence on Security Innovation (CSI), Sponsored by Comcast, University of Connecticut
11/12-08/13 Charles H. Knapp Associate Professor in Electrical Engineering, University of Connecticut
04/12-11/12 F.L. Castleman Associate Professor in Engineering Innovation, University of Connecticut
08/08-08/11 Term member of Graduate Faculty, ECE Department, Duke University
08/10-08/13 Associate Professor, Electrical and Computer Department, University of Connecticut
08/06-08/10 Assistant Professor, Electrical and Computer Department, University of Connecticut
08/04-08/06 Assistant Professor, Department of Computer Science and Electrical Engineering (CSEE), University of Maryland Baltimore

Non-academic Appointments

2020-2023 President and CTO, Caspia Technologies, A UF Spin-off Technology Company,
<http://caspiaTechnologies.com/>

Fundraising (Endowments and Gifts) - ~\$50M

1. Comcast Center of Excellence, \$12M

2. Gifts and donation from TESCAN, ZEISS, and FEI valued about \$12M
3. Research Gifts from Cisco, LMCO, Ansys, ADI, and other companies, \$4M
4. Citi Innovation Partnership for Advanced Information and Intelligent technologies, \$3M
5. Sachio Semmoto Chair of Electrical and Computer Engineering, \$3M
6. Wally Rhines Professorship in Semiconductor, \$1M
7. Wally Rhines Professorship in Quantum Engineering, \$1M
8. Wally Rhines Professorship in Hardware Security, \$1M
9. Wally Rhines, Department Excellence Fund, \$200K
10. Chris Malachowsky, Wndowed professorship Fund, \$2M
11. James Spoto estate gift + Conference Room naming, \$4.5M
12. RC GonzalesEstate fund to establish an Endowed Professorship, faculty fellow, and student scholarship, \$1.5M
13. James Spoto, ECE Headquarter Meeting Room, \$125K
14. 2x Kent and Linda Fuchs Faculty Fellow, \$200K
15. Chuck Kung, \$250K
16. Alan Hasting, Endowed Professorship plus addional fund for his faculty fellow, \$1.1M
17. Michael Hsing Faculty Fellow, \$100K
18. MPS Equipment Donation and Cash Gifts, \$1M
19. H. Michael Gach Endowed Fund, \$300K
20. Women in ECE (WECE) Endowment Fund, \$200K
21. David B. Vozolla ECE Department Innovation Fund + Undergraduate research support, \$135K
22. Neil Katz, Naming Advising Office, \$100K
23. Ann and Tim Chen, 2x Faculty Fellow + Naming a Conference Room in MALA, \$275K

Major Initiatives and Accomplishments

2025-present	Led establishing the Annual Iranian-Aperican Pioneers (IAP) Summit
2025-present	Led establishing FL ECE Chairs annual event, including 13 ECE department from across the state of Florida
2024-present	ECE Global Initiative: This initiative established presence for FL ECE in every continent (Southeast Asia, Middle East, Europe, Africa, and South America).
2022-2025	Alumni Engagement: Established a comprehensive plan for alumni engagement. This includes estabdisning ECE Hall of Fame, Distinguished Alumni, Alumni mentorsnp, and more.
2024-2025	Quantum Initiative: Started a statewide quantum initiative called Florida Alliance for Quantum Technology (FAQT), brought 15 schools together, signed an MOU between all 15 schools and the state of Florida. This is considered the largest initiative among all schools in the state of Florida. In addition, established a \$1M endowment in addition to adding 2 new faculty to the quantum team. Finally. we're in the process of applying for institute designation for this initiative. https://faqt-florida.org/
Dec. 2024	Japan-US Semiconductor Security Initiative. This initiative is meant to increase collaboration between US and Japan. Next step is to provide
Dec. 2023	Semiconductor Initiative: Led FL State Semiconductor Initiative (\$80M+ investment). As of Dec. 2024, a total of \$150M funding came to the department in the semiconductor area. https://www.flgov.com/2024/01/26/governor-ron-desantis-celebrates-successful-semiconductor-investments-calls-for-more-support-in-legislative-session/
July 2023	UK-US Semiconductor Security Initiative. This initiative started in 2022 in collaboration with my UK counterparts. We assembled officials from both sides to come together in Washington DC to discuss ways to collaborate on semiconductor security. Attendess from department of Defense, homeland security, CHIPS, NIST, DARPA, SRC, DSTI, UK Ministry of Science, and

	more. We are now in the process identifying funding (\$\$M) to support this initiative through SRC and DSIT.
Feb. 2023	Established New Teaching Policy: A clear policy with regard to teaching assignment and course load, approved by the faculty.
July 2022	Established Southeast Consortium on Assured and Leading-Edge Semiconductors (SCALES) - http://scales-consortium.org/
June 2022	Established Florida Semiconductor Institute (FSI) – This was the first initiative in my role as chair of the ECE department.
June 2022	Increase collaboration between College of Medicine and the ECE department. This has resulted in exponential increase the ECE department submission to NIH.
June 2022	Planned for top 10 public ranking with clear set of outcomes: Increase collaboration: multi-department, multi-college; Increase center-oriented research: Planned for 5 centers of excellence; Young faculty mentoring and development; Establish large partnership with industry; Planned underway to increase research expenditure; Path-to-Full for Associate Professors; Modernizing undergraduate laboratories; Increase faculty honorifics; Increase PhD graduation rate; Improve Diversity, Equity, and Inclusion (DEI); Improve AA ranking; Industry remote PhD
Oct. 2021	Established a workshop between UF and USF to enable more collaboration between researchers in the field of cybersecurity.
April 2021	FICS TDC 2021: A virtual conference was established to enable demonstration of the technologies developed in FICS to the sponsors
Sept 2020	Established CAR, Center for Aerospace Resilience , in collaboration with Embry-Riddle Aeronautical University (ERAU) sponsored by FL DOE, and serves in collaboration with Dr. Remzi Seker of ERAU. \$1.75M (no indirect)
August 2020	Ranked #3 in the entire University of Florida funding in 2019-2020 fiscal year with my portion of fund of almost \$15M. The top two faculty were from Medical Schools. Note the total funding of UF in 2019-2020 fiscal year was \$900M.
July 2020	Established the first certificate on Hardware Security offered through MEST Center . This certificate includes none hours of presentation on nine topics in the domain of hardware security.
May 2020	Teamed up with Synopsys as Prime to successfully compete on DARPA Automated Implementation of Secure Silicon (AISS) BAA . Synopsys was awarded \$48M, of which FICS will receive \$8M. Other team members include Boeing, ARM, UC San Diego, Purdue University, and Texas A&M.
April 2020	Established Edaptive Computing Inc. Transition Center (ECI-TC), \$15M+ , This unique partnership between the University of Florida (UF) and Edaptive Computing has two main goals. Firstly, the proposed center will continue the groundbreaking work taking place in FICS Research—using automation, computer vision, and machine learning to test and verify the designs of microelectronics in all phases of the lifecycle. This work is fundamentally aimed at verifying that hardware (IoT devices, chips, circuit boards, systems) has been manufactured to the exact specifications of the designers, that the system does not suffer from any hardware related vulnerabilities, and that the designs themselves have not been compromised in any way. These efforts to ascertain the trustworthiness of devices entering the supply chain have become increasingly critical as more and more manufacturing has moved to East Asia, where oversight is less stringent. https://news.ece.ufl.edu/2020/04/29/15m-technology-transition-center-kicks-off-virtually/
Feb 2020	Founder, President, and CTO, Caspia Technologies, LLC. http://caspiaTechnologies.com/
June 2019	Led the establishment of the National MicroElectronic Security Training (MEST) Center , Sponsored by OSD/AFRL/Navy (https://mestcenter.org/). This center mission is to establish collaboration between multiple universities, establishing an ecosystem of training modules and options to suit the need for diverse government and industry employees, place strong emphasis on

- hands-on learning, offer major courses and certificate programs, Provide comprehensive coverage of all security topics, Offering major courses and certificate programs, unique in the nation, and establish self-learning kits for hardware and systems security topic available for remote training and busy professionals.
- May 2019 Led establishment of **AFOSR/AFRL Center of Excellence** on Enabling Cyber Defense in Analog and Mixed Signal Domain (**CYAN**). This center focuses on identifying opportunities in the analog and mixed signal domain to establish end to end security for electronic devices and systems.
- March 2019 Led the **2019 FICS Research Annual Conference on Cybersecurity** (<https://fics.institute.ufl.edu/conference/>). 180 people attended the conference from academia, industry, and government. The event was sponsored by 11 companies.
- Nov. 2018 Co-authored the **first ever textbook** on Hardware Security, published by Morgan Kaufman <https://www.elsevier.com/books/hardware-security/bhunia/978-0-12-812477-2>
- Feb 2018 Led the **2018 FICS Research Annual Conference on Cybersecurity** (<http://fics-institute.org/outreach/conference/>). More than 230 people attended the conference from academia, industry, and government. The event was sponsored by 18 companies.
- Aug 2017 Established a program to increase the number of student awards and scholarships (NSF, SRC, IBM, etc.) among faculty and FICS Research students.
- Aug 2017 Led establishing the **Trusted and Assured MicroElectronics (TAME) Forum** (<http://www.tameforum.org/>). TAME Forum's objective is to provide a bi-annual platform to researchers in academia, and practitioners in industry and government to discuss innovative solutions in the domain of trusted microelectronics in today's globalized and complex supply chain, discuss grand challenges and identify collaboration opportunities. One major outcome of the TAME Forum is expected to be the first ever "National Technology Roadmap for Trusted and Assured Microelectronics".
- Dec. 2017 Co-founded IEEE **PAINE (International Conference on Physical Attacks and Inspection of Electronic Systems)**. <http://paine-conference.org/>
- Aug 2017 ACR: Established **ECE Faculty Mentoring Program**. This program is intended to build a strong foundation for the success of junior faculty (assistant and associate professors). Many new faculty have had little or no exposure to the different and new aspects of their profession, and desire an experienced voice to guide them in tailoring the initial stages of a successful career. It is critical to continually provide opportunities for career development through a strong voluntary mentor/mentee relationship. As a result, we established flexible career guidance and mentoring program to create a nurturing environment within the ECE department.
- June 2017 **Proposal Writing and Review Process**: Instituted a CAREER/PECASE/YIP proposal writing review process internally for the ECE Department. Through this program, young faculty in the ECE department received NSF CAREER, YIP, and PECASE awards.
- March 2017 Led the **2017 FICS Research Annual Conference on Cybersecurity** (<http://fics-institute.org/outreach/conference/>). More than 210 attended the conference from academia, industry, and government. The event was supported by 13 companies, more than 20 demos and 50 posters were presented, with many companies and government labs active in recruiting students for full time and summer intern positions.
- Jan 2017 Led establishing **CyberGatorZ**, and currently serving as the faculty advisor. CyberGatorZ is a fully student-run organization at the FICS Research Institute. CyberGatorZ group includes four major committees namely Incident Analysis and Reporting, IoT Hacking, Outreach and Diversity, and Professional Development. CyberGators mission is to advance the state of art in cybersecurity and increase students professional development by providing opportunities to communicate with experts from academia, industry, and government. CyberGatorZ are also active members of the K-12 initiative run by FICS Research.
- Dec. 2016 Worked closely with the lead PI Prof. Bhunia on an **NSF Scholarship for Service (SFS)**. The accepted proposal, in collaboration with FIU, received \$4.6M to recruit BS, MS and PhD

- students for a new program called *Hardware and Systems Security (HSS)* jointly developed at the UF ECE/CISE and FIU ECE department. The target program will be made available online through UF EDGE (online) program. The EDGE capability will allow FIU students to take the basic HSS classes and then continue with other cybersecurity courses in their respective departments. The program is available nation wide to all students from ECE, CSE, ME, BME, and other departments.
- August 2016 Led establishment of **SCAN Lab under FICS Research Institute**. The lab includes \$10M+ equipment with capabilities for physical inspection, imaging capabilities, attack assessment, electrical tests and measurement, bio-medical tests, thermal test, device characterization, etc.
- April 2016 The topic of hardware security has seen major growth over the past decade or so. However, the community never enjoyed a dedicated journal on this topic, hence my colleague Prof. Bhunia and I took on this challenge and established the first ever journal supported by Springer called **Journal of Hardware and Systems Security (HASS)**, <http://www.editorialmanager.com/hass>
- April 2016 Helped establish **IEEE Symposium on Asian Hardware-Oriented Security and Trust (AsianHOST)**. AsianHOST Symposium brings together experts from Asia, Europe and North America together to establish collaboration on topics related to Hardware Security. <http://asianhost.org/>
- Feb 2016 **UF-TESCAN Partnership**: Led this effort to establish a partnership with one of the leading electron microscope companies in the world. This partnership is worth about \$5M. The partnership includes significant donation, 5-year warranty, monthly meeting with TESCAN to develop strategies for collaboration and joint proposals to government and industry, student training, joint publications, etc. <http://fics.institute.ufl.edu/facilities/>
- Feb 2016 Led the establishment of the **2016 FICS Annual Conference on Cybersecurity**. The goal of this conference was to put together a program consisting of experts from industry, government, and academia to discuss cybersecurity problems, engage with students via poster sessions and evaluation, project demos, panels, competitions, etc. The first year event brought together more than 155 experts on campus. The 2016 conference was sponsored by more than 12 companies. <http://fics.institute.ufl.edu/conference/>
- July 2015 Led establishing the **Florida Institute for Cybersecurity (FICS) Research** to become a premier institute on cybersecurity that covers device to systems, human, mobile, network, software, and enterprise security. <http://fics.institute.ufl.edu/>
- Nov. 2015 **CDC Tool** became part of **SAE international standard, AS6171**. The CDC project was sponsored in part by Honeywell, Comcast, and Missile Defense Agency (MDA). The tool is the first of its kind to evaluate the efficiency of test and inspection techniques for counterfeit and fake chips. *The tool was acquired by SAE International.*
- April 2015 Initiated **Connecticut Cybersecurity Center (C3)** at the University of Connecticut. I led a proposal for a total of \$1M+ funded by the State of Connecticut. The fund allowed for recruiting two new faculty and a full time staff. <https://ccc.engr.uconn.edu/>
- Nov 2014 Helped with the effort to establish a **Center of Excellence in Microscopy** at the University of Connecticut. This is a multi million dollar (\$20M+) partnership between UConn and FEI. <http://today.uconn.edu/blog/2014/10/new-collaboration-to-create-world-class-microscopy-center/>
- Oct. 2014 Led establishment of **CyberSEED (Cybersecurity, Education, and Diversity Challenge Week)**. <http://www.csi.uconn.edu/cybersecurity-week>. CyberSEED, supported by more than a dozen companies, brought together students (undergraduate and graduate) from more than 45 schools and colleges around the nation to compete on many cybersecurity problems on campus at UConn. The students competed on capture the flag (CTF), software security, and hardware security.
- May 2014 **Lead PI for MURI grant from DOD AFOSR**. The U.S. Department of Defense awarded a \$8.5 million grant to the University of Connecticut, University of Maryland, and Rice University to support research that will analyze and upgrade security protections for nanoscale computer

hardware. UCONN with 6 PIs is the lead institution and University of Maryland (2PIs) and Rice University (1 PI) are the other collaborators. <http://news.engr.uconn.edu/muri-grant-to-improve-the-security-of-nanoscale-computer-devices.php>. **This was the single largest grant brought to the University of Connecticut.**

- April 2014 **Founding Director for CSI Center at UConn:** In partnership with Comcast, I led the establishment of the **Center of Excellence in Security Innovation (CSI)**. The CSI was established to lead research, teaching and workforce development in hardware, software, and network security and address Comcast's much needed security needs. CSI was established in April 2014 with main support from Comcast (\$2M/year). <http://www.csi.uconn.edu/>
- June 2012 Established the **Center for Hardware Assurance, Security, and Engineering (CHASE)**. The Center was established in 2012 to provide the University of Connecticut with a physical and intellectual environment necessary for interdisciplinary hardware-oriented research and applications to meet the challenges of the future in the field of assurance and security. CHASE is a research consortium with member companies from across the nation committed to enabling knowledge breakthroughs that shape future electronic systems. Current members include Honeywell, Comcast, Missile Defense Agency (MDA), and Juniper Networks. Other sponsors include Synokey, LSI, Qualcomm, Cisco, Samsung, Mangolia, R3Logic, Freescale, SRC, GRC, and more. <https://www.chase.uconn.edu/>
- Feb. 2012 Established a series of **Workshops on Hardware and Systems Security at UConn**. The workshop grew quite fast that went from *60 participants in 2012* to *220 in 2014*. We were able to bring together experts from academia, industry, and government to discuss the challenging problems of hardware and cyber security.
- Feb 2011 Led establishment of **Trust-Hub** (www.trust-hub.org) funded by the National Science Foundation (NSF). Trust-Hub is a website where members of the IC hardware security community can share their discoveries and other information that accelerates hardware security research and developments. Trust-Hub serves as a clearing house and community-building tool where researchers can exchange papers, benchmarks, hardware platforms, source codes and tools.
- Jan 2008 Led the establishment of the IEEE Workshop on **Hardware-Oriented Security and Trust (HOST)**, with Dr. Jim Plusquellic of UNM. In 2010, HOST became a symposium and is now the premier event on hardware security. HOST moved to Washington DC area in 2013 and grew to become an event with more than 350 attendees by 2017. <http://www.hostsymposium.org/>
- 2006-present Published the **first series of books on Hardware Security and Trust**. Two of the books is currently being used as text book in the domain of hardware security and translated into multiple language including Korean and Chinese. <http://tehranipoor.ece.ufl.edu/publications.html>

Education

- 1/02 – 8/04 Ph.D, Electrical and Computer Eng., University of Texas at Dallas, 2002-2004
- 9/97 – 8/00 M.Sc. Electrical Engineering, University of Tehran, 1997-2000
- 1/92 – 8/97 B.Sc. Electrical Engineering, Tehran Polytechnic University, 1992-1997

Project Sponsors

1. National Science Foundation (NSF)
2. Semiconductor Research Corporation (SRC)
3. Global Research Corporation (GRC)
4. National Institute of Standards and Technology (NIST)
5. Office of Naval Research (ONR)
6. Army Research Office (ARO)
7. Air Force Research Laboratory (AFRL)
8. Air Force Base Eglin
9. Missile Defense Agency (MDA)

10. GAANN, Department of Education
11. Defense Advanced Research Projects Agency (DARPA)
12. Air Force Office of Scientific Research (AFOSR) – MURI
13. KCP, Department of Energy (DOE)
14. AFOSR / DURIP
15. OSD/ONR SBIR
16. DRAPER
17. Raytheon
18. Tektronix
19. Texas Instruments
20. Cisco
21. Qualcomm
22. LSI Corporation
23. Freescale Semiconductor
24. MediaTek
25. Comcast
26. Honeywell
27. Juniper
28. BRIDG
29. Mentor Graphics
30. Intel
31. R3Logic
32. Synokey
33. UF Office of Research
34. CRI/Rambus Donation
35. Verigy, Inc. Donation
36. Xilinx Donation
37. Agilent Donation
38. EPSRC of United Kingdom
39. UConn Research Foundation
40. UMBC RAS/RIS
41. EYL Partners & Korean Institute for Information, Communication Technology Promotion (IITP)
42. Edaptive Computing Inc.
43. Bosch
44. Nimbis Services
45. Analog Devices (ADI)
46. DMEA
47. AFWERX
48. Dynetics
49. Battelle
50. Lockheed Martin
51. Synopsys
52. Department of Education (DOE), FL
53. Ansys
54. Arm
55. Meta (Facebook)
56. NSA
57. FL DOE
58. NSF ENGINE
59. State of FL
60. National Security Research Institute (NSRI), Korea

61. MPS

62. *Small donations/Services:*

- IBM
- Intel
- Raytheon
- Draper
- TESCO
- ZEISS
- Thales E-security
- Texas Instruments
- Rambus
- Mentor Graphics
- NREL
- Hamamatsu
- Microphotonics
- Cisco
- Angstrom Scientific
- Cybraics
- Athena Groups
- Raith
- Bruker
- United Technology Research Center
- Microsemi
- Applied DNA Sciences
- Micronet Solutions
- PFP Technologies
- ARA
- Edaptive Computing
- Synopsys
- Onespinn
- Battelle
- Arm
- Riscure

Research Supports and Donations (PI and Co-PI), \$240M+

2025	MPS, GenAI based Analog Component Selection and Analysis, 100K, Lead PI
2025	Semiconductor Research Corporation (SRC), PASS: Physically-Aware Secure Software Execution, \$315K, Lead PI
2024-2025	National Security Research Institute, South Korea, \$100K, PI
2024	State of Florida Semiconductor Initiative, \$80M (Collaboratively with many stakeholders)
2024	NSF ENGINE, up to ~\$26M, co-PI
2024	State of FL, Semiconductor Initiative, \$80M
2023	DURIP: Dual Beam Laser Interferometry and Ferroelectric Analysis for Physical Assurance of In-Memory Computing and Sensing Technologies, \$290K, AFOSR, Co-PI
2023	MRI: Track 2 Acquisition of a Novel Performance-Driven 3D Imaging System for Extremely Noisy Objects (NPIX), NSF, \$2.5M, Co-PI
2023	DARPA NGMM: Next Generation Microelectronics Manufacturing, \$2M, Lead by: BRIDG
2022-2025	AutoMap: Automated Mapping of Security Properties, SRC, \$270K, Co-PI
2022-2025	An Evolutionary AI-Based Fuzz Testing for Extensive SoC Security Verification, SRC, \$270K, PI

2022-2025	Intelligent Detection and Mitigation of Hardware and Firmware Attacks for Resilient Unmanned Aircraft Systems, NSA, 600K, Co-PI
2022	Synopsys ZeBu Emulation Unit for Advanced Emulation-based SoC Security Verification (Zeus), AFOSR DURIP, \$290K, Co-PI
2022	Analog Devices, Security Enginer Assessment, \$150K, Lead PI
2022	AFB Egin, Inter-layer PCB Impaging and Assurance, Lead PI, \$330K
2022	Cisco, FPGA Bitstream Protection Against Optical Attacks, Co-PI, \$200K
2021	Scanning Acoustic Microscope for Advanced Packaging Physical Assurance (SAPPA), \$280K, ONR, Co-PI
2021	Facebook gift, \$75K, co-PI
2021	Synopsys gift, \$65K, PI
2021-2023	Extensible Secure SoC Architectures, SRC-Arm, \$200K, Co-PI
2021-2024	SAIPA: Security Aware Interposer Design for Heterogeneous Packaging, ONR, \$900K, Co-PI
2020-2021	Model-based PCB Attestation, KC-NSC, \$150K, Co-PI
2021-2022	SHINE: Security Aware High-Level Synthesis, DARPA, \$500K, Co-PI
2020-2021	TrustGuard: Trusted Embedded Systems using Power Side Channel Signal Analysis, ADI, \$100K, gift, Co-PI
2020-2023	Fault Injection Assessment, ANSYS, Co-PI, \$120K, gift
2020-2021	Center for Aerospace Resilience (CAR), DOE FL, \$1,750,000, Co-PI, Co-director
2020-2021	Secure Assessment of AI Hardware and Accelerators, AFOSR, \$1M, Lead PI
2020-2021	PCB Assurance Using Multi-Modal Data Infusion Based on Vulnerability/Risk Analysis, Cisco, \$100K, Co-PI
2020-2021	A Holistic Approach for PCB Physical Inspection Using Learning Based Methods, Cisco, \$100K, Co-PI
2020-2023	CCRI: ENS: Collaborative Research: Trust-Hub: Development of Benchmarks, Tools, Metrics, and Validation Platforms for Hardware Security, and a Web-based Dissemination Portal, NSF, \$1.8M, Lead PI
2020-2021	PCB Assurance Using Multi-Modal Data Infusion Based on Vulnerability/Risk Analysis, Cisco, Co-PI, \$100K
2020-2021	A Holistic Approach for PCB Physical Inspection Using Learning Based Methods, Cisco, Co-PI, \$100K
2019-2023	DARP AISS ABIL – AISS By Industry Leaders, DARPA, ~\$8M, Lead PI for UF FICS (Total: \$48M)
2020	SBIR Navy, collaborate with Edaptive
20202-2022	Blockchain-Enabled Electronic Supply Chain Security, Nimbis Services, \$1.1M, Lead PI
2020-2022	Hardware Vulnerability Ontology and Database for the Trusted Silicon Stratus, Battelle, HVD/HVO, \$1.1M, Co-PI
2020-2021	Security Analysis and Implementation of DOSC Architecture, DARPA, \$680K, Lead PI
2020-2021	ECI-TC Project on PCB and IC Assurance, \$1.35M
2020	Lockheed Martin, Gift, \$50K
2020-2023	STAMP: A Holistic Backward/Forward Trust Framework for Protecting Microelectronics Throughout Lifecycle, AFRL, \$5.4M, Lead PI
2020-2022	Automated Delaying-Image Capture System (ADICS), MicroNet/DMEA, \$300K, co-PI
2019	Ultra Backside Thinning of Integrated Circuits for Physical Assurance and Inspection, AFOSR DURIP, \$290K, Lead PI
2019-2020	Side Channel Attack Testbench Emulator (SCATE), DARPA, \$150K, Co-PI
2019-2022	CAD Framework for Analyzing and Mitigating Security Vulnerabilities in High-level Synthesis Flow, SRC, \$250K, Lead PI
2019-2020	Microelectronics Security, Analog Devices, \$90K, Lead PI
2019-2032	National Microelectronics Security Training Center (MEST), \$27M, Lead PI

2019-2021	HARDEN: Hardware-Assisted ML-based Anomaly Detection for Cyber Defense, Cisco, \$175K, Lead PI
2019-2021	HAWKS: Hardware Knowledge-Oriented Software Security Verification, Cisco, \$200K, Co-PI
2019-2022	Pre-Silicon Security Verification and Backside Protection Schemes for Microelectronic Devices, AvMC/Dynetics, \$2.15M, Lead PI
2019	Analog Devices, Establishing FICS Speaker Series on Cybersecurity, \$15K, Gift, Lead
2019	Test Vehicle Design for HT Detection Validation, KCP Honeywell, \$91K, Co-PI
2019-2020	Design Security Rule Check for SoCs, DARPA, \$420K, Lead PI
2019-2024	University Center of Excellence: CYAN: Enabling Cyber Defense in Analog and Mixed Signal Domain, AFOSR/AFRL, \$8.4M (with cost share), Co-directors: Waleed Khalil and Mark Tehranipoor
2019	AI Based Dynamic Encoding and Encryption Optimizer Powered by Quantum Entropy Chip, AFWERX Challenge on Microelectronic Design, \$1.2M, Co-PI
2019-2020	ISIP: A Comprehensive Framework for Information Security for Intellectual Property and System-on-Chip Verification, Cisco, \$100K, Lead PI
2019	Automated In-situ Large-area De-processing of ICs with High Throughput Electronic, STTR with Navid Asadi, DMEA / MicroNet Solutions, \$44K, Co-PI
2019-2021	AutoBoM: Intelligent Framework for Automated Bill of Material Generation and Physical Inspection of PCBs, Edaptive / AFRL, \$3M+, Lead PI
2019	Hardware Security Assessment, Bosch, \$36K, Lead PI
2018-2021	Disciplined Microarchitectural Side Channel Detection, Intel, \$165K (+ Option Years 2 and 3, Total: ~\$500K), Co-PI
2018-2021	STV: Automated SoC Trust Validation Using Dynamic Trojan Benchmark Generation, Penn Test, and Deep Learning, Edaptive Computing, \$1.4M, Lead PI
2018-2019	Protecting Obfuscated Circuits against Attacks that Utilize Test Infrastructure, DARPA, \$380K, Lead PI
2018-2021	A Holistic Approach for Device to System Authentication, Air Force Eglin, \$300K, PI
2018-2021	A Framework for Scalable Software Integrity Verification on Clear Hardware Assumptions, Texas Instruments/SRC, \$450K, co-PI
2018-2021	EMLA: Metrics and Tools for Automated EM-Leakage Analysis at Pre-Silicon, NIST, \$260K, Co-PI
2018-2021	Developing Firmware Security Testing Technology for IoT Devices, Korean Institute for Information and Communication Technology Promotion, Co-PI, Total: \$2.54M, UF Share: ~\$600K
2018-2019	BRAND: A Basic Framework for PCB Reverse Engineering, Analysis, and Defect Diagnosis, Cisco, \$100K, Co-PI
2018	ARA, \$10K
2018	2018 FICS conference support, \$42K
2018-2019	A Framework for Automatic Detection of Fault Attack Vulnerabilities, Cisco, \$100K, Co-PI
2018-2019	CRI/Rambus, DPA/EM Workstation, Donation, \$187K Lead PI
2018-2019	DURIP, ONR Nano-probing Integrated Circuits for Physical Attacks and Hardware Security Assessment, ONR, Co-PI, \$285K
2017-2018	MRI: Acquisition of a High-Resolution Photon Emission/Electro-Optical Microscope for Non-invasive Evaluation of Electronic Devices and Systems Security, NSF, Lead PI, \$1M + \$400K Cost Share from UF
2017-2020	NSF-SRC STARSS, SaTC: STARSS: Small: iPROBE - An Internal Shielding Approach for Protecting against Frontside and Backside Probing Attacks, Co-PI, \$440K
2017-2019	Hardware IP Protection through Provably Secure State-Space Obfuscation, DARPA, Co-PI, \$560K
2017-2018	PHASE II: FORTIS: Establishing Forward Trust for Protecting IPs and ICs in Today's Complex Supply Chain, Cisco, \$100K, Co-PI

2017-2019	A Comprehensive Framework for IoT Security and Privacy Evaluation Through Quantitative Metric, Cisco, \$220K, IoT Vulnerability Database, Co-PI,
2017-2018	PHASE II: Scalable Hardware Trojan Detection using Statistical Test Generation and Side Channel Analysis, Raytheon, \$100K, Co-PI
2017-2018	PHASE II: A Framework for Automatic Fine-Grain Timing Attack Vulnerability Evaluation, Draper, \$20K, Co-PI
2017-2020	ASiLA: Automated Side-Channel Leakage Analysis: Metrics and Tools, NIST, \$500K, Lead PI
2017	2017 FICS conference sponsorship, \$28K
2017-2019	Security Validation of Integrated Circuits by Detailed Parameter Analysis Using Probe Station, ARO DURIP, \$250K, Lead PI
2017-2018	Test Chip Design for Evaluating Trust, Honeywell, Lead PI, \$210K
2017-2022	NSF SFS, SURPASS: NSF SFS Unique Scholarship Program in Hardware and Systems Security, Co-PI, \$6.2M
2016-2018	Design Security Rule Check, SRC, Lead PI, \$200K
2016-2019	Utilizing NIST Entropy as a Service and Chaotic Circuits for Management of Electronic Component Supply Chain, National Institute of Standards and Technologies (NIST), Co-PI, \$500K
2016-2017	Timing Side-channel Analysis of Integrated Circuits, Draper, Co-PI, \$50K
2016-2017	Self-referencing in Space and Time for Golden-Free Hardware Trojan Detection, Raytheon, Co-PI, \$100K
2016	2016 FICS Conference support, \$25K
2016	Donation from Tektronix (electrical test instruments), \$150K
2016-2019	Establishing HACE (Hardware Security, Attack, and Countermeasure Evaluation Lab) Lab, NSF SaTC Education, PI, \$300K
2016-2017	Gift from Intel for purchasing Servers and Workstations, \$50K
2016-2019	Combating Counterfeit Analog and Mixed Signal ICs with Lightweight Embedded Mechanisms and Innovative Electrical Tests, NSF, Co-PI, \$400K
2016	In-kind Contribution for ZEISS Orion, ZEISS, \$1M
2016	Precise nano-fabrication and advanced circuit edit, DURIP, AFOSR, Lead PI, \$1M
2016	TESCAN, in-kind contribution and gift to establishing INSPECT center at UF, \$2.2M
2016-2018	Led the effort for establishing collaboration between FICS and Cisco in three areas: (1) IP Security and Trust, (2) Design for Security, and (3) Establishing forward trust from 3PIP to OEM, Cisco, Research Gift, \$500K
2015-2018	Computer Systems Security, GAANN program, Department of Education (DOE), \$591K, Co-director
2015-2018	CI-EN: Trust-Hub: Development of Benchmarks, Metrics, and Validation Platforms for Hardware Security, and a Web-based Dissemination Portal, NSF, Lead PI, \$1.56M
2015-2017	Connecticut Cybersecurity Center (C3), State of Connecticut, Lead PI, \$1M
2015	Security Rule Check: A Comprehensive Framework for Evaluating Security of Integrated Circuits, Semiconductor Research Corporation (SRC), Lead PI, \$100K
2015-2018	REU Site: Research Experience in Cyber and Civil Infrastructure Security for Students with ADHD: Fostering Innovation, NSF, Co-PI, \$344K
2014	2014 CHASE/CSI conference support + CyberSEED, \$350K
2014-2019	Development of Universal Security Theory for Evaluation and Design of New Nanoscale Devices, DOD/AFOSR MURI, Lead PI, \$7.5M
2014-2017	SHF:Small: GOALI: Advanced Physical Inspection of Counterfeit Integrated Circuits, NSF GOALI, Co-PI, \$425K
2014-2017	Design of Low-Cost Memory-Based Security Primitives and Techniques for High-Volume Products, NSF/SRC STARSS, Lead PI, \$460K
2014-2015	CHASE Membership, Juniper, Platinum Membership, \$140K

2014	SBIR: Detecting Malicious Circuits in IP Cores, Office of Secretary of Defense (OSD), Co-PI, \$150K
2013	2013 CHASE conference support, \$30K
2014-2017	Comcast Center of Excellence in Security Innovation (CSI), \$10M, Founding Director
2014-2017	Hardware Security and Security Assessment, Comcast, Lead PI, \$185K
2014	Server Infrastructure, Donation to CHASE by Comcast, \$300K
2013-2014	Physical Inspection equipment, Tech Park, \$1M
2013-2014	Test Time Reduction for SOC's, LSI, Sole PI, \$25K
2012	2012 CHASE workshop support, \$20K
2013	Electrical Test Equipment, Tech Park, \$140K
2013-2016	Low-Cost Self-Test Solutions for Improving Test Quality and Device Reliability and Resiliency, SRC, Sole PI, \$300K
2013-2014	Comcast Lab, Hardware Security Assessment, Comcast, Lead PI, \$285K
2013-2014	Equipment donation, Comcast, Lead PI, \$170K
2013-2015	CHASE Membership, Honeywell, Platinum Membership, \$200K
2013-2015	CHASE Membership, Comcast, Platinum Membership, \$200K
2013-2014	Memory-based Physical Unclonable Function (PUF), Synokey, \$90K
2013-2016	Development of Innovative Solutions for Hardware Security, and Detection and Prevention of Counterfeit Electronics Components, Missile Defense Agency (MDA), Sole PI, CHASE Funding, Platinum Membership, \$292K
2013-2015	DOD IASP grant, Co-PI, \$141K
2013-2014	Improving Hardware Security and Trust, Comcast, Lead PI, \$93K
2013-2014	New Low-Cost LBIST for Improving Test Quality, GRC, Sole PI, \$35K
2013-2016	A Multi-Level Test Approach for Improving Reliability and Performance of Nanometer Technology Designs, NSF/SRC, \$270K, Sole PI, \$270K
2012-2013	Technique to Measure Voltage Noise during Structural and Functional Testing of ASICs, Cisco, Sole PI (Gift, no indirect cost), \$60K
2012-2015	Computer Systems Security, GAANN, Dept. of Education, (Co-PI), \$400K
2013-2015	Efficient Test for Power Switches in Digital SOC's, EPSRC, Travel Grant to Southampton, UK, \$10K
2012-2013	ARO Special Workshop on Counterfeit Electronics, \$30K
2012-2013	Improving Security and Trustworthiness of IC Supply Chain, Comcast, \$96K
2012-2013	CAREER: Novel Techniques for Detecting and Localizing Hardware Trojans in Integrated Circuits, NSF REU, \$16K
2012-2013	High Quality Delay Tests for Nanometer Technology Designs, MediaTek, Sole PI (Gift, no indirect cost), \$45K
2011-2014	Collaborative Research: CI-ADDO-NEW: Trust-Hub: Design of Trust Benchmarks, Hardware Validation Platforms and a Web-based Dissemination Portal, Lead PI, \$1,230,000, NSF, \$1.23M
2011-2014	Design-for-Hardware-Trust Techniques, Detection Strategies and Metrics for Hardware Trojans, Sole PI, Army Research office (ARO), \$240K
2011-2012	Analysis and Measurement of Aging Effects on Circuit Performance in Nanometer Technology Designs, Cisco, Sole PI (Gift, no indirect cost), \$60K
2011-2014	Exploratory Curriculum for Trustable Computing Systems Security Education (Co-PI), NSF, \$200K
2011-2012	Correlating Structural Fmax with Functional Fmax, Qualcomm (Gift, no indirect cost), \$30K
2011	Xilinx Equipment Donation, \$5K
2010-2011	Effective Reliability and Variability Analysis of Sub-45nm Designs for Improving Yield and Product Quality, Cisco, Sole PI (Gift, no indirect cost), \$60K
2011-2014	REU: Trustable Computing Systems Security Research and Education, NSF, (one of 5 PIs), \$350K
2011-2012	UConn Intermediate Grant (one of 6 PIs), \$99K

2010-2013	Test and Analysis for Critical Reliability and Variability Paths for Improving Yield, Product Quality and Reliability, Semiconductor Research Corporation (SRC), Sole PI, \$300K
2010-2012	Collaborative Research: CI-ADDO-NEW: Trust-Hub: Design of Trust Benchmarks, Hardware Validation Platforms and a Web-based Dissemination Portal, NSF Planning Grant, Lead PI, \$100K
2010	Agilent Equipment Donation, \$40K
2010, 2011	Xilinx Equipment Donation, \$10K
2010-2011	In-kind donation for Ocelot ZFP Tester, Verigy, \$315K
2009-2014	CAREER: Novel Techniques for Detecting and Localizing Hardware Trojans in Integrated Circuits, NSF, Sole PI, \$400K
2009-2012	Reliable Systems Design at Below 45-nm Technologies, SRC Custom Research, Freescale, Sole PI, \$165K
2009-2012	Computer System Security, GAANN, Dept. of Education, (Co-PI), \$525K
2009-2010	ARO Special Workshop on Hardware Assurance, Sole PI, \$25K
2009-2013	High Quality Delay Test for VDSM Designs, LSI Logics, Sole PI, \$150K
2009-2010	Root Cause of Timing Defects, Mentor Graphics, Sole PI, \$43K
2008-2009	Intel Equipment Grant, Sole PI, \$25K
2008-2012	GOALI (Industry-University Collaborative Project): Collaborative Research: Scalable Techniques for Detecting Small-Delay Defects in Nanometer Integrated Circuits, NSF, PI, \$400K
2008-2012	CPA-DA: Dealing with Voltage Variations and Supply Noise During Performance Verification in Nanometer Technology Designs, NSF, Sole PI, \$250K
2008-2009	Silicon Design Authentication and Malicious Alteration Detection in Integrated Circuits Using Delay Analysis, UConn Research Foundation, Sole PI, \$24K
2007-2010	Collaborative Research: Detection and Isolation of Malicious Inclusions in Secure Hardware (DIMINISH), NSF, Lead PI, \$300K
2007-2010	Timing-Aware ATPG for Maximizing Crosstalk/Signal Integrity on SOCs, Semiconductor Research Corporation (SRC), Sole PI, \$282K
2005-2008	At-Speed Transition Fault Testing Using Low Cost Testers, SRC Custom Research, Texas Instruments, Sole PI, \$152K
2005-2006	Frequency Driven Buffer Insertion (RAS, UMBC), \$10K, PI
2005-2006	Securing Designs Against Non-Invasive Attacks (RAS, UMBC), \$20K, PI

Industry Experience

1/98 – 11/01 **Advanced DSP Research Center, SAM Communications**
 Designing emulator boards for TMS320C54x DSP, Implementing different programs on 'C54x emulator, internal memory BIST and implementation on 'C54x DSP.

In the Press

DAC Cast: Mark Tehranipoor Confronts his Cyber Adversaries Intelligently

<https://audio.com/erik-seligman/audio/daccast16-tehranipoor>

AI: A New Tool For hackers and For Preventing Attacks, Semi Engineering,

<https://semiengineering.com/ai-a-new-tool-for-hackers-and-for-preventing-attacks/>

Interview with Siemens

Design Automation Takeaways, <https://semiwiki.com/events/357672-caspia-focuses-security-requirements-at-dac/>

Florida Semiconductor Week convenes leaders to strengthen and expand Florida's semiconductor manufacturing ecosystem

<https://news.ufl.edu/2024/02/florida-semiconductor-week/>

Semiconductor Research Corporation Recognizes Innovation and Excellence at their 25th TECHCON Networking Event

<https://statics.teams.cdn.office.net/evergreen-assets/safelinks/1/atp-safelinks.html>

The Threat of Supply Chain Insecurity

<https://semiengineering.com/the-threat-of-supply-chain-insecurity/>

Testing Chips for Security

<https://semiengineering.com/testing-chips-for-security/>

Is There a Practical Test for Rowhammer Vulnerability

<https://semiengineering.com/is-there-a-practical-test-for-rowhammer-vulnerability/>

Florida Trend: The one big threat when it comes to cyber-security has nothing to do with software

<https://www.floridatrend.com/article/31635/the-one-big-threat-when-it-comes-to-cyber-security-has-nothing-to-do-with-software>

CNN: Raid of former Florida Covid data scientist's home could affect other state employees, legal experts warn

<https://www.cnn.com/2020/12/08/us/rebekah-jones-whistleblower-raid-invs/index.html>

University of Florida Researcher Creates Innovative Training Platform That Makes Cyberspace a Safer Place (UF Innovate)

<http://innovate.research.ufl.edu/2020/11/10/tehranipoor-si2020-story/>

UF researchers thrive despite the pandemic

https://www.alligator.org/news/uf-researchers-thrive-despite-the-pandemic/article_90c863e2-eb38-11ea-b3b1-bbc6f8f7bdf7.html

Interview with Semicon 2020

<https://blog.semi.org/technology-trends/industry-expert-qa-the-key-to-chip-security-trust-and-verify-but-how>

IEEE Spectrum Recognizes Dr. Tehranipoor's technology at:

<https://spectrum.ieee.org/computing/hardware/three-ways-to-hack-a-printed-circuit-board>

University of Florida hits record \$900 million in research awards

<https://news.ufl.edu/2020/08/record-research-awards/>

FICS Research Receives \$7.8M to Help Make On-Chip Security Pervasive

<https://news.ece.ufl.edu/2020/05/13/tehranipoor-darpa-aiss/>

Playing Digital Defense, Florida High Tech Corridor

<https://floridahightech.com/playing-digital-defense/>

This Tech Would Have Spotted the Secret Chinese Chip in Seconds: University of Florida Researchers use X-rays, optical imaging, and AI to spot spy chips in computer systems

<https://spectrum.ieee.org/riskfactor/computing/hardware/this-tech-would-have-spotted-the-secret-chinese-chip-in-seconds>

Interview with New York Times

Interview with the Florida Trend, Connected World

Vulnerability Note VU#739007

<http://www.kb.cert.org/vuls/id/739007>

Crypto Bugs in IEEE Standard Expose Intellectual Property in Plaintext

<https://www.bleepingcomputer.com/news/security/crypto-bugs-in-ieee-standard-expose-intellectual-property-in-plaintext/>

Flaws in IEEE P1735 electronics standard expose intellectual property

<http://securityaffairs.co/wordpress/65184/hacking/ieee-p1735-electronics-standard-flaws.html>

IEEE Spectrum, M. Tehranipoor, U. Guin, and S. Bhunia, "Invasion of the Hardware Snatchers: Fake Hardware Could Open the Door to Malicious Malware and Critical Failure," IEEE Spectrum, 2017.

<http://spectrum.ieee.org/computing/hardware/invasion-of-the-hardware-snatchers-cloned-electronics-pollute-the-market>

UF's Annual Cybersecurity Conference Focuses on Security of IoT

<https://www.eng.ufl.edu/newengineer/ece/fics-2017/>

Interview with Le Monde France: Fight against counterfeit electronic components

http://www.lemonde.fr/sciences/article/2016/12/05/lutter-contre-la-contrefaçon-de-composants-electroniques_5043610_1650684.html

Pensacola News Journal: Cybersecurity must increase with automation

<http://www.pnj.com/story/money/business/2016/11/28/cybersecurity-must-increase-automation/94546842/>

UF Partners with TESCAN to create world-class hardware security lab

<http://www.strategic-directions.com/a/industry-news/?action=2&terms=&sdi=26f5e7d4-b522-47e8-8c6e-63a1474edbf>

University of Florida Cybersecurity Team Turns to Tektronix to Outfit Electronics Security Lab

<http://finance.yahoo.com/news/university-florida-cybersecurity-team-turns-130000458.html>

WUFT, Nov. 15, 2015, Cybersecurity Discussion Raises Concern For Experts

<http://www.wuft.org/news/2015/11/15/cybersecurity-discussion-raises-concern-for-experts/>

Cyber-security at Florida's public and private universities

<http://www.floridatrend.com/article/19478/cyber-security-at-floridas-public-and-private-universities>

IEEE Spectrum

<http://spectrum.ieee.org/tech-talk/telecom/security/an-unhackable-qr-code-to-fight-bogus-chips>

BusinessWire:

NIST Cybersecurity advisor visited CHASE center, Feb. 2014.

http://www.businesswire.com/news/home/20150219005203/en/NIST-Cybersecurity-Chief-Discuss-Threats-Framework-Implementation#.VOX_2MYsO8l

Yahoo Finance:

<http://finance.yahoo.com/news/university-connecticut-comcast-sponsor-first-130000543.html>

Washington Times

<http://www.washingtontimes.com/news/2014/apr/29/universities-to-research-nanotechnology-security/>

Wall Street Journal

<http://online.wsj.com/article/PR-CO-20140410-912537.html>

Universities beef up cybersecurity, identity theft research

<http://gcn.com/blogs/pulse/2014/04/ut-uconn-cybersecurity-research.aspx>

Credit Card Data Theft: Stopping the Hackers

<http://today.uconn.edu/blog/2014/03/credit-card-data-theft-stopping-the-hackers/>

Expert Discusses Steps to Address Threat of Cyber Attacks

<http://today.uconn.edu/blog/2013/10/expert-discusses-steps-to-address-threat-of-cyber-attacks/>

Cover Story, IEEE Spectrum, The Hidden Dangers of Chop-Shop Electronics

<http://spectrum.ieee.org/semiconductors/processors/the-hidden-dangers-of-chopshop-electronics>

Conference on Counterfeit Electronics Addresses Growing National Concern

<http://www.chase.uconn.edu/conference-on-counterfeit-electronics-addresses-growing-national-concern.php>

Sen. Lieberman Praises UConn Cybersecurity Labs

<http://today.uconn.edu/blog/2012/02/sen-lieberman-praises-uconn-cybersecurity-labs/>

Lieberman pushes for cyber security

<http://www.dailycampus.com/news/lieberman-pushes-for-cyber-security-1.2794957#.T1P6RvEgdGM>

Research Initiative Will Enhance Integrity of Integrated Circuits

<http://today.uconn.edu/?p=34063>

University of Connecticut and Duke University Develop Unique Method to Improve Testing for Small Delay Defects in Semiconductors

<http://www.hartfordbusiness.com/news14048.html>

<http://www.physorg.com/news199362652.html>

http://www.advn.com/news_University-of-Connecticut-and-Duke-University-Develop-Unique-Method-to-Improve-T_43665962.html

<http://www.forbes.com/feeds/businesswire/2010/07/20/businesswire142648135.html>

<http://www.src.org/newsroom/press-release/2010/86/>

NYU-Poly and UConn Researchers Develop New Design Techniques to Protect Against Vulnerabilities in the Electronics Supply Chain

<http://www.marketwatch.com/story/student-hackers-and-a-dose-of-skepticism-secure-vital-hardware-2011-11-08>

Xuehui Zhang Received First Place Prize at the 2010 CSAW - Embedded Systems Challenge

http://www.brooklyneagle.com/categories/category.php?category_id=31&id=39204

<http://www.poly.edu/press-release/2010/11/02/who-will-protect-our-digital-future-woman-high-school-videographer-student->

Interview with “The Economist”

Interview with EBN

Interview with NPR (twice)

Interview with WUFT

Academic Awards & Honors

2026	IEEE Computer Society Taylor L. Booth Education Award , for outstanding leadership in hardware security education, development of large-scale training programs, composing pioneering textbooks, and novel curriculum development
2025	Fellow , Artificial Intelligence Industry Alliance
2025	FSI Founder’s Award , for setting the vision and laying the groundwork for the Florida Semiconductor Institute
2025	Best Paper , A System-Aware Remote Fault-Injection Attack Detection & Mitigation for Secure Heterogeneous Systems, IEEE HOST
2025	Best Paper Candidate , NoXLock: SiP Activation and Licensing through Obfuscated On-Chip Network and Fuzzy Traffic, the Asia and South Pacific Design Automation Conference (ASP-DAC)
2024	Best Paper Candidate , ChiPICA: Chiplet Physical Inspection Certification Authority for Trust Verification in Heterogeneous Integration, IEEE PAINE
2024	Best Poster Candidate , CAKE-SiP: Chiplet Authenticate & Key Exchange for Secure Provisioning in System-in-Package, IEEE PAINE
2024	Honorable Mention , RC-FSM-G: Automatic Security Rule Checking for Finite State Machine at the Netlist Abstraction, International Test Conference (ITC)
2024	Best Paper Candidate , Continuity in Security: Leveraging LLM for Translating Security Properties Across Hardware Designs,” Int. Conference on Very Large-Scale Integration (VLSI-SoC)
2024	Fellow , Asia-Pacific Artificial Intelligence Association (AAIA)
2024	Best Paper Candidate, ML-Based Optimal Virtual Placement Exploration for EM Side-Channel Mitigation , DesignCon
2023	SRC Aristotle Award (https://www.src.org/award/aristotle/)
2023	Best Paper Candidate, SoCFuzzer: SoC Vulnerability Detection using Cost Function enabled Fuzz Testing , Design Automation and Test in Europe (DATE)
2023	Best Paper Candidate, EvoLUTe: Evaluation of Look-Up-Table-Based Fine Grained IP Redaction , Design Automation and Test in Europe (DATE)
2023	Best Paper Candidate, RTLlock: IP Protection using Scan-Aware Logic Locking at RTL , Design Automation and Test in Europe (DATE)
2023	Fellow , National Academy of Inventors (NAI)
2022	IEEE Computer Society TTTC Bob Madge Innovation Award

2022	Best WiP Paper Award, K. Zamiri Azar, H. Kermani Mardani, F. Farahmandi, and M. Tehranipoor, “ Warm up before Circuit De-obfuscation? An Exploration of the Possibilities ” IEEE HOST, 2022
2021	ACM Fellow
2020	Teacher/Scholar of the year , Herbert Wertheim College of Engineering, University of Florida
2020	The paper titled “ SHADE: Automated Refinement of PCB Component Estimates Using Detected Shadows ,” received the best student paper award in IEEE Conference on Physical Assurance and Inspection of Electronics (PAINE), 2020.
2020	Ranked #3 among all PIs at the University of Florida in awarded funding for 2020
2020	Received Inventor of the Year Award from UF Innovate ; Technology highlighted during the Standing InnOvation Event in September 2020
2018	Inducted into HOST Hall of Fame
2018	Best Paper Award , K. Xiao, D. Forte, Y. Jin, R. Karri, S. Bhunia, M. Tehranipoor, “Hardware Trojans: Lessons Learned after One Decade of Research,” ACM Transaction on Design Automation of Electronic Systems (TODAES), 2017
2018	IEEE Fellow
2017	Outstanding Paper Award , E. L. Principe, N. Asadizanjani, D. Forte, M. Tehranipoor, R. Chivas, M. DiBattista, S. Silverman, M. Marsh, J. Mastovich, J. Odum, “ Steps Towards Automated Deprocessing of Integrated Circuits ,” International Symposium on Test and Failure Analysis (ISTFA), 2017
2017	College of Engineering Excellence in Leadership Award , University of Florida
2017	ECE Research Excellence Award , ECE Department, University of Florida
2017	Best Paper Award , X. Wang, Y. Guo, T. Rahman, D. Zhang, and M. Tehranipoor, “ DOST: Dynamically Obfuscated Wrapper for Split Test against IC Piracy ,” IEEE Asian Hardware-Oriented Security and Trust Symposium (AsianHOST), 2017.
2017	The article “ Hardware Trojans: Lessons Learned After One Decade of Research ” published in IEEE Transactions on Design Automation of Electronic Systems (TODAES) was included the 21st Annual Best of Computing (http://www.computingreviews.com/recommend/bestof/notableitems.cfm?bestYear=2016).
2016	TTTC Most Successful Event Award for HOST Symposium , Co-founded by Tehranipoor
2016	Best Paper Award , Q. Shi, N. Asadi, D. Forte, and M. Tehranipoor, “ A Layout-driven Framework to Assess Vulnerability of ICs to Microprobing Attacks ,” IEEE Symposium on Hardware-Oriented Security and Trust (HOST), 2016.
2016	Best Paper Candidate , K. Yang, D. Forte, and M. Tehranipoor, “ UCR: An Unclonable Chipless RFID Tag ,” IEEE Symposium on Hardware-Oriented Security and Trust (HOST), 2016.
2015	Best Paper Award , “K. Xiao, D. Forte, and M. Tehranipoor, “ Efficient and Secure Split Manufacturing via Obfuscated Built-In Self-Authentication ,” IEEE Hardware-Oriented Security and Trust (HOST), 2015”
2015	The paper titled “ Counterfeit Integrated Circuits: Detection, Avoidance, and the Challenges Ahead ” was recognized by JETTA as the most downloaded article in 2014
2015-present	Intel Charles E. Young Preeminence Endowed Professor in Cybersecurity, University of Florida
2015-present	Elected member of Connecticut Academy and Science and Engineering (CASE)
Nov. 2014	ISE North America, US and Canada, Best Project finalist for establishing CHASE and CSI centers
Nov. 2014	Best paper Candidate , International Symposium on Test and Failure Analysis (ISTFA), 2014
Oct. 2014	ISE Northeast, Best Project finalist for establishing CHASE and CSI centers
Aug 2014	Air Force Office of Scientific Research (AFOR) MURI Award (2014-2019)
Sep. 2014	UConn ECE Research Excellence Award
2012- 2014	Charles Knapp Associate Professor

May 2013	Best Paper Award , IEEE North Atlantic Test Workshop (NATW), 2013
2012	IEEE Computer Society Golden Core Inductee
Oct. 2012	Best Student Paper Award , IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems (DFT), 2012
2011- 2012	F.L. Castleman Associate Professor in Engineering Innovation
June 2012	IEEE Computer Society Outstanding Contribution Award
April 2012	SOE Outstanding Faculty Advisor Award
Jan 2012	Best Special Session Award, IEEE VLSI Test Symposium (VTS), 2011
2010-2013	IEEE Computer Society Distinguished Speaker
2010-2013	ACM Distinguished Speaker
May 2010	Recipient of the IEEE Computer Society TTTC Most Successful Technical Event for founding HOST Symposium
May 2010	Recipient of the 2009 IEEE Computer Society Certificate of Appreciation
May 2009	UConn ECE Research Excellence Award, 2009
Jan. 2009	NSF CAREER Award , 2009
May 2009	Best Paper Award , IEEE North Atlantic Test Workshop, 2009
Oct. 2008	IEEE Computer Society Meritorious Service Award , 2008
May 2008	Best Paper Award , IEEE North Atlantic Test Workshop, 2008
May 2008	Honorable Mention for Best Paper Award , IEEE North Atlantic Test Workshop, 2008
May 2007	Best Panel Award , IEEE VLSI Test Symposium (VTS), 2006
Nov. 2006	Top Ten Recognition Paper , ITC 2005
March 2006	Best Paper Award , IEEE VLSI Test Symposium (VTS), 2005
April 2006	Best Paper Candidate , Design Automation Conference, 2006
Sep. 2005	Best Paper Candidate , TI Symposium on Test (TIST), 2005
1/02 – 08/04	Received Texas Public Educational Grant, 2002-2004
July 1997	Ranked 2nd , Undergraduate Program, ECE Department, Tehran Polytechnic University
June 1992	Ranked 1st , High School, Among all high school students in Golestan province, Iran

Students Awards for their Projects under my Supervision

- My PhD student Nitin Pundir received the Best Dissertation Recognition Award, Title: **Security Verification for SoC Designs**, IEEE HOST 2022
- The Demo called **eChain: A Blockchain Based Ecosystem for Trusted Electronic Devices** won the Attendee's Choice Award, IEEE HOST 2022
- Team **Gator Hardware Oriented Security team (GHOST)** won first prize in IEEE HOST 2022 Microelectronic Security Challenge (IP Security Track).
- Andrew Stern received the 3rd place in the **2021 IEEE TTTC McCluskey Best Doctoral Thesis Award**
- Huanyu Wang received the 2nd place in the **2021 IEEE TTTC McCluskey Best Doctoral Thesis Award**
- The **Hardware Demo presented in HOST-2020** called "SPARTA: Laser Probing Approach for Trojan Detection" Received the judges best demo award
- The **Hardware Demo presented in HOST-2020** called "FPGA-As-A-Service Security" Received the attendees best demo award
- Andrew Stern received the second Prize for his hardware demo on "**Utilizing EM Emanation for Provenance Analysis of Microelectronic Devices**", IEEE International HOST, May 2018, Washington DC
- Andrew Stern, Received **best demo award** at the FICS 2018
- Fahim Rahman, Received **best poster award** at the FICS 2018
- Huanyu Wang, Received **best poster award** at the FICS 2018

- **Best Poster Award supported by DRAPER**, Andrew Stern, Haoting Shen, Xiaolin Xu, Domenic Forte, Mark Tehranipoor, **Near Field EM for Foundry of Origin Identification**, 2017 FICS Annual Conference on Cybersecurity
- **Best Poster Award**, Gustavo K. Contreras, Adib Nahiyen, Domenic Forte, Mark Tehranipoor, **Track and Extract: Information Flow Tracking for Security Vulnerability Analysis and Exploit Extraction**, 2017 FICS Annual Conference on Cybersecurity
- **Best Poster Award**, Troy Bryant, Sreeja Chowdhury, Domenic Forte, Mark Tehranipoor, Nima Maghari, **An All-Digital PUF (Physically Unclonable Functions) for AMS Applications Using Stochastic Comparator Voltage Offset**, 2017 FICS Annual Conference on Cybersecurity
- Adib Nahiyen and Gus Contreras receive **Best Poster Award** at the 2016 FICS Annual Conference on Cybersecurity, Title: **DSeRC: Design Security Rule Check**
- Mehdi Sadi received **Best in Session Award** from TECHCON, 2016 for his paper titled **BIST-Assisted In-field Aging Reliability Management of SoCs Using On-Chip Clock Sweeping and Machine Learning**
- G. Contreras received **Best in Session Award** from TECHCON, 2016 for his paper titled **Fault Deterministic Vector Analysis and Seed Extraction for LBIST**
- Tauhid Rahman received **Best in Session Award** from TECHCON, 2016 for his paper titled **SRAM Inspired Design and Optimization for Developing Robust Security Primitives**
- **Qihang Shi** received the Best TA Award from the ECE Department, UConn, 2012
- **Andrew Ferraiuolo, Adam Zimmer, and Rifat Chowdhury** won the first prize from ECE on their Senior Design Project under my supervision, 2012
- **Nicholas Tuzzio, Xuehui Zhang and Andrew Ferraiuolo**: Received the first place prize at the 2011 CSAW - Embedded Systems Challenge (Physical Unclonable Functions)
- **Xuehui Zhang, Nicholas Tuzzio, and Andrew Ferraiuolo**: Received the third place prize at the 2011 CSAW - Embedded Systems Challenge (Malicious Processor Design)
- **Junxia Ma**: Selected as one of the four finalists for Connecticut Women of Innovation (WOI)
- **Brian Helfer, Theodore Estwan, and Emilio Cepeda** won the first prize from ECE on their Senior Design Project under my supervision, 2011
- **Xuehui Zhang**: Received First Place Prize at the 2010 CSAW - Embedded Systems Challenge
- **Michel Wang**: Received Best in Session Award at TECHCON 2010
- **Nisar Ahmed**: Received UConn SOE Outstanding Graduate Thesis Award
- **Joseph Larosa, Corey Benoit, Andrew Tan, and Kevin Perkins** won the first prize from ECE on their Senior Design Project under my supervision, 2010
- **Junxia Ma**: Received Best in Session Award at TECHCON 2009
- **Jeremy Lee**: Received the TTTC Best Thesis Research Poster Award, 2008
- **Jeremy Lee**: Received the Best Computer Engineering Seminar Presentation, 2008
- **Paul Rago and Aaron Feldstein** won the second prize from ECE on their Senior Design Project under my supervision, 2008
- **Nisar Ahmed**: Received the TTTC 2007 Best Doctoral Dissertation Award
- **Kevin Tyler, Danny Ho, and Vimal Vachhani** won the first prize from ECE on their Senior Design Project under my supervision, 2007
- **Nisar Ahmed**: Received the UMBC-CSEE's Best PhD Thesis Award, 2006

Professional Activities

Founding Positions:

- **Co-founder**, IEEE International Physical Attacks and Inspection on Electronics (**PAINE**) Conference <http://paine-conference.org/>
- **Founder**, Trusted and Assured Microelectronics Forum (**TAME**) www.tameforum.org
- **Co-founder**, Journal of Hardware and Systems Security (**HASS**), 2016

- <http://www.editorialmanager.com/hass>
- **Co-founder**, IEEE Asian Symposium on Hardware-Oriented Security and Trust (**AsianHOST**), 2016
<http://asianhost.org/index.htm>
- **Co-founder**, International Verification and Security Workshop (**IVSW**) and member of the steering committee,
<http://tima.imag.fr/conferences/ivsw/ivsw16/>
- **Founder and Director**, Florida Institute for Cybersecurity (**FICS**), 2015-present
<http://www.institute.ufl.edu>
- **Founding Director**, Center for Hardware Assurance, Security, and Engineering (**CHASE**), 2012-2015
<http://www.chase.uconn.edu/>
- **Founding Director**, Comcast Center of Excellence in Security Innovation (**CSI**), 2013-2015
<http://www.csi.uconn.edu/>
- **Co-founder**, IEEE Int. Symposium on Hardware-Oriented Security and Trust (**HOST**), 2008
<http://www.engr.uconn.edu/HOST/>
- **Co-founder**, Trust-Hub, 2010
<http://www.trust-hub.org/>

IEEE/ACM Events Chair Positions:

- **Co-general Chair**, IEEE International Symposium on Hardware-Oriented Security and Trust (HOST), 2024
- **Co-general Chair**, IEEE International Symposium on Hardware-Oriented Security and Trust (HOST), 2022
- **Vice-Program Chair**, IEEE International Workshop on Silicon Lifecycle Management (SLM), 2021
- **Co-general Chair**, IEEE International Hardware-Oriented Security and Trust (HOST) Summit, 2021
- **General Chair**, IEEE International Physical Assurance and Inspection of Electronics (PAINE) Conference, 2019, 2020, 2021
- **General Chair**, CAD4Sec Workshop, Co-located with DAC, 2022
- **Program Chair**, International Test Conference (ITC), 2019
- **Editor-in-Chief**, Journal of Hardware and Systems Security (HASS), 2016-present
- **Associate EIC**, IEEE Design & Test of Computers, 2012-2014
- **IEEE CS Fellow Evaluation Committee**, IEEE CS, 2018-2022
- **IEEE Cybersecurity Initiative Ambassador** (2016-2020)
- **Vice-program Chair**, International Test Conference (ITC), 2018
- **Co-Program Chair**, International Verification and Security Workshop (IVSW), 2016
- **Co-Program Chair**, IoT and Automotive Security Workshop (ISAW), 2017
- **Co-program Chair**, IEEE International Workshop on Cross-Layer Cyber-Physical Systems Security (CPSS), 2016
- **Co-program Chair**, IoT Security Workshop, co-located with IEEE HOST 2017
- **Vice-General Chair**, IEEE North Atlantic Test Workshop (NATW), 2011
- **General Chair**, IEEE Workshop on Defect and Data Driven Testing (D3T), 2009, Austin, TX
- **General Chair**, IEEE International Symposium on Defect and Fault Tolerance of VLSI Systems (DFT), 2009, Chicago, IL
- **General Chair**, IEEE International Symposium on Hardware-Oriented Security and Trust (HOST), 2009, San Francisco, CA
- **General Chair**, 1st IEEE International Symposium on Hardware-Oriented Security and Trust (HOST), 2008, Anaheim, CA
- **Steering Committee Chair**, IEEE International Symposium on Hardware-Oriented Security and Trust (HOST), 2008-present
- **Program Chair**, IEEE Workshop on Defect Based Testing (DBT), 2008, Santa Clara, CA
- **Program Chair**, IEEE International Symposium on Defect and Fault Tolerance of VLSI Systems (DFT), 2008, Boston, MA

- **Program Chair**, IEEE Workshop on Defect Based Testing (DBT), 2007, Santa Clara, CA
- **Local Arrangement Chair**, IEEE Int. Symp. on Defect and Fault Tolerance in VLSI Systems (DFT), 2006, Washington DC
- **Member, Steering Committee**, IEEE Workshop on Defect and Data Driven Testing (D3T), 2009-2010
- **Chair**, Hardware Security Subcommittee, Design Automation Conference (DAC), 2019, 2020
- **Member, Steering Committee**, International Test Conference (ITC), 2018-present
- **Member, Steering Committee**, IEEE Workshop on Defect and Adaptive Test Analysis (DATA), 2011-present
- **Member, Steering Committee**, IEEE International Verification and Security Workshop (IVSW), 2016-present
- **Vice-Chair**, TTTC Technical Activity group on Hardware Security and Trust
- **Vice-General Chair**, IEEE North Atlantic Test Workshop (NATW), 2012
- **Co-program Chair**, Internet of Things (IoT) and Automotive Security Workshop (IASW), co-located with HOST Symposium, 2017-present
- **Industry Liaison**, IEEE International Symposium on Hardware-Oriented Security and Trust (HOST), 2014-present
- **Industry Liaison**, Workshop for Women in Hardware and Systems Security (WISE), 2017-present
- **Industry Liaison**, IEEE Asian Symposium on Hardware-Oriented Security and Trust (AsianHOST), 2016
- **Panel Chair**, IEEE Asian Symposium on Hardware-Oriented Security and Trust (AsianHOST), 2016-present
- **Security Special Session Track Chair**, IEEE International Microprocessor Test and Verification (MTV) conference, 2016
- **Security Track Co-chair**, International Test Conference (ITC), 2016-present
- **Security Track Chair**, Design Automation Conference (DAC), 2017-2018
- **Design Automation Conference (DAC) Security Special Focus Committee, 2018-2019**
- **Steering Committee**, Attacks and Solutions in Hardware Security (ASHES), Co-located with CCS 2017-present
- **Exhibit Chair**, IEEE International Hardware-Oriented Security and Trust (HOST), 2020

Non-IEEE Events Chair Positions and Memberships:

- **Workshop Chair**, NATCAST workshop on Hardware Security, UF, August 2025
- **Member**, Florida Semiconductor Institute (FSI) Advisory Board
- **Co-Program Chair**, UK-US Semiconductor Security Initiative, Nov. 2023
- **Member**, Scientific Advisory Board, Center for Advanced Studies, LMU Munich
- **Chair**, Advisory Board, SECURE Center. Prairie View A&M University (PVAMU)
- **Florida State University System (SUS) Cybersecurity Steering Group (Governing Council)**, 2020-present
- **Co-Chair**, Trusted and Assured Microelectronics (TAME) Forum, Nov. 2017
- **Steering Committee**, Trusted and Assured Microelectronics (TAME) Forum
- **Chair**, FICS Annual Conference on Cybersecurity, March 2017. **13 companies sponsored this event. 210 attended.**
- **Chair**, FICS Annual Conference on Cybersecurity, February 2016. **12 companies sponsored this event. 155 attended.**
- **Chair**, CHASE Conference on Secure/Trustworthy Systems and Supply Chain Assurance, 2015. **10 companies sponsored this event.**
- **Co-organizer**, CyberSEED (<http://www.csi.uconn.edu/cybersecurity-week>), **More than a dozen companies sponsored this event.**
- **Chair**, CHASE Workshop on Secure/Trustworthy Systems and Supply Chain Assurance, 2014 (<https://www.chase.uconn.edu/chase-workshop-2014.php>). **8 companies sponsored this event.**
- **Chair**, ARO/CHASE Sponsored Workshop on Counterfeit Electronics, 2013

- **Chair**, 2nd ARO Sponsored Workshop on Hardware Assurance, 2011
- **Chair**, 1st ARO Workshop on Hardware Assurance, 2009

Editorial Board:

- **Associate Editor**, IEEE Transactions on Computers, 2019-2022
- **Associate Editor**, IEEE Transactions on VLSI (**TVLSI**), 2015-2022
- **Associate Editor**, ACM Transactions on Design Automation of Electronic Systems (**TODAES**), 2013-2020
- **Associate Editor**, IEEE Design & Test of Computer Magazine, 2009-2015, 2020-2021
- **Associate Editor**, Journal of Low Power Electronics (**JOLPE**), 2009-2022
- **Associate Editor**, Journal of Electronic Testing: Theory and Applications (**JETTA**), 2007-2022
- **Editor**, Test Technology Technical Council (**TTTC**) Newsletter, 2008-2011

Guest Editor:

- Special issue on CAD for Security: Pre-silicon Security Sign-off Solutions Through Design Cycle, ACM Journal on Emerging Technologies in Computing Systems (**JETC**), 2022, F. Farahmandi, A. Srivastava, G. Di Natale, and M. Tehranipoor
- Special issue on Physical Assurance and Inspection of Electronics, Springer Journal on Hardware and Systems Security (**HaSS**), 2020, N. Asadi, and M. Tehranipoor
- C. Chang, M. van Dijk, U. Ruhrmair, and M. Tehranipoor, Emerging Attacks and Solutions for Secure Hardware in the Internet of Things, IEEE Transactions on Dependable and Secure Computing (**TDSC**), May/June 2019
- IEEE Transactions on Multi-Scale Computing Systems, Special Issue on Hardware/Software Cross-Layer Technologies for Trustworthy and Secure Computing, Shiyang Hu (Michigan Technological University), Yier Jin (University of Central Florida), Mark M. Tehranipoor (University of Connecticut), Kenneth Heffner (Honeywell)
- IET Computers and Digital Techniques, Special Issue on Hardware Security, Ilia Polian (U of Passau) and M. Tehranipoor (UConn), 2013-2014
- Special issue on "On-chip Structures for Smarter Silicon", IEEE Design & Test of Computers, Co-guest Editor: LeRoy Winemberg (Freescale Semiconductor), 2012
- IEEE Computer Society (**CS**) Computing Now on Hardware Security and Trust, September 2010
- IEEE Design & Test Special Issue on "Verifying Physical Trustworthiness of Integrated Circuits and Systems", Co-guest Editor: Farinaz Koushanfar (Rice University), 2009
- Special issue on "Test, Defect Tolerance, and Reliability of Nanoscale Devices", Journal of Electronic Testing: Theory and Applications (**JETTA**), 2007
- Special issue on "IR-Drop and power Supply Noise Effects on Design and Test of Very Deep Submicron Designs", IEEE Design & Test of Computers, Co-guest Editor: Ken Butler (Texas Instruments), 2008

Tutorials

- IEEE International Hardware-Oriented Security and Trust (**HOST**), **Secure Heterogeneous Integration**, May 2023
- International Test Conference (ITC), CAD for **SoC Security Verification**, September. 2022
- IEEE International Hardware-Oriented Security and Trust (**HOST**), **CAD Solutions for SoC Security**, June 2022
- Design, Automation, and Test in Europe (**DATE**), CAD for SoC Security, Feb. 2022
- International Test Conference (ITC), **SoC Security Verification**, Oct. 2021
- IEEE International Hardware-Oriented Security and Trust (**HOST**), **CAD Solutions for SoC Security**, Dec. 12, 2021
- Design, Automation, and Test in Europe (**DATE**), CAD for SoC Security, Feb. 2021
- IEEE International Hardware-Oriented Security and Trust (**HOST**), **CAD for SoC Security**, Dec. 2020

- IEEE International Hardware-Oriented Security and Trust (**HOST**), **CAD for SoC Security**, Washington DC, May 2019
- IEEE International Hardware-Oriented Security and Trust (**HOST**), **Protecting Electronics Supply Chain from Throughout Lifecycle**, Washington DC, May 2018
- IEEE International Hardware-Oriented Security and Trust (**HOST**), **Protecting Electronics Supply Chain from Design to Resign**, Washington DC, May 2017
- International Test Conference (ITC), **Test Opportunities and Challenges for Secure Hardware and Verifying Trust in Integrated Circuits**, Dallas/Fort Worth, TX, 2016
- **Dagstuhl Seminar on Hardware Security**, Germany, Dagstuhl, 2016, Title: Hardware Security (<http://www.dagstuhl.de/de/programm/kalender/semhp/?seminr=16202>)
- International Test Conference (ITC), **Test Opportunities and Challenges for Secure Hardware and Verifying Trust in Integrated Circuits**, 2015
- Design Automation Conference (DAC), **Introduction to Hardware Security**, M. Potkonjak (UCLA), M. Tehranipoor (UConn), 2015
- IEEE International System-on-Chip Conference (SOCC), **Electronic Component Supply Chain Security: Threats, Challenges, and Solution**, M. Tehranipoor (UConn), 2014
- Design, Automation, and Test in Europe (DATE), **All You Need to Know About Hardware Trojans and Counterfeit ICs**, M. Tehranipoor and D. Forte (UConn), 2014
- IEEE Conference on VLSI, 2014, **All You Need to Know About Hardware Trojans and Counterfeit ICs**, M. Tehranipoor and D. Forte (UConn)
- IEEE International Reliability Physics Symposium (IRPS), 2013, **Chip to System Reliability Fundamentals**, M. Tehranipoor (UConn), Nemat Bidokhti (Cisco), and Bill Eklow (Cisco)
- International Test Conference (ITC), 2011, **Testing Low-Power Integrated Circuits: Challenges, Solutions, and Industry Practices**, Srivaths Ravi (Texas Instruments), M. Tehranipoor (UConn), and Rohit Kapur (Synopsys)
- International Test Conference (ITC), 2011, **High-Quality and Low-Cost Delay Testing for VDSM Designs: Challenges & Solutions**, M. Tehranipoor (UConn), Krish Chakrabarty (Duke University), and Jeff Rearick (AMD)
- Design Automation Conference (DAC), 2011, **Chip to System Reliability Fundamentals**, M. Tehranipoor (UConn), Nemat Bidokhti (Cisco), and Bill Eklow (Cisco)
- International Test Conference (ITC), 2010, **Testing Low-Power Integrated Circuits: Challenges, Solutions, and Industry Practices**, Srivaths Ravi (Texas Instruments), M. Tehranipoor (UConn), and Rohit Kapur (Synopsys)
- International Test Conference (ITC), 2010, **High-Quality and Low-Cost Delay Testing for VDSM Designs: Challenges & Solutions**, M. Tehranipoor (UConn), Krish Chakrabarty (Duke University), and Jeff Rearick (AMD)
- Design, Automation, and Test in Europe (DATE), 2010, **Testing Low-Power Integrated Circuits: Challenges, Solutions, and Industry Practices**, Srivaths Ravi (Texas Instruments), M. Tehranipoor (UConn), Rohit Kapur (Synopsys)
- International Conference on VLSI Design, Title: **High-Quality and Low-Cost Delay Test for VDSM Designs**, January 2009
- **IEEE MidWest Symposium on Circuits and Systems**, Title: High-Quality Delay Tests for Nanometer Technology Designs, August 2008

Panelist

- Panel Moderator, GenAI for Security or Security for GenAI? A SoC Design Perspective, AI/CAD4Sec Workshop, co-located with DAC 2025
- Panelist: Design Automation Conference (**DAC**) Pavilion Panel, From Design to Defense: Shaping the future of Microelectronics Security, June 2024

- Panelist: International Test Conference (**ITC**), 2023, Panel: Grand Test Challenges
- Panelist: IEEE GLS-VLSI, Hardware Security in the Post-CHIPS Era, 2023
- Panelist: IEEE Workshop on Silicon Lifecycle Management (**SLM**), 2021
- Panelist: Microelectronics Security, Raytheon RX ISaC Technology Network Panel, May 2021
- Panel Co-moderator, High Level Synthesis: Facts, Myths, and fantasies, IEEE HOST, Dec. 2020
- Panelist: Quantifiable Assurance, IEEE **HOST** 2020
- Panelist: Hardware Security, SRC SIA DOE workshop on Decadal Plan for Semiconductors workshop on ICT Hardware Enabled Security
- Panelist: Education and Workforce Development, ERI Summit, August 2020
- Panelist: Assured AI, Trusted and Assured Microelectronic (**TAME**) Forum, Washington DC, May 2019
- Panelist: Hardware Supply Chain Security in Asia and Around the World, IEEE AsianHOST, 2018
- Panelist: Trusted and Assured Microelectronics (**TAME**), Vision for TAME (co-located with HOST), May 2018
- Panel Moderator with Edna Conway, Women in Hardware and Systems Security Workshop (**WISE**), May 2018
- Panelist, Global Electronic Supply Chain: What Can South East Asian do about it? IEEE **AsianHOST**, 2017
- Panelist: Internet of Things (IoT) and Automotive Security Workshop (**IASW**), 2017
- Panelist: NYU Alfred P. Sloan Foundation, Cybersecurity Lecture, with Wally Rhines, Chairman and CEO of Mentor Graphics, April 2017
- Panelist: International Workshop on Hardware Security, 2016, Title: Research Collaboration Opportunities in Hardware Security Areas
- Panelist: IEEE VLSI Test Symposium (**VTS**), 2016, Title: Test Challenges for Secure Hardware
- Panelist: International Symposium on Quality Electronic Design (**ISQED**), 2016, Title: Hardware and Systems Security Challenges in IoT Era
- Panelist: FIU Cybersecurity Conference, October, 2015
- Panelist: IEEE VLSI Test Symposium (**VTS**), 2015
- Panelist: IEEE S&P Symposium, San Jose, CA, May 2014
- Panelist: SRC STARSS, San Jose, CA, May 2014
- Panelist: Microprocessor Test and verification (**MTV**), Nov. 2013
- Panelist: IEEE North Atlantic Test Workshop (**NATW**), May 2013
- Panelist: Cisco innovation Test Conference (**CITC**), 2012
- Panelist: International Workshop on Defect and Adaptive Test Analysis (**DATA**), September 2011
- Panelist: International Test Conference (**ITC**), November 2010
- Panelist: IEEE Symposium on Hardware-Oriented Security and Trust (**HOST**), June 2010
- Panelist: International Test Conference (**ITC**), Nov. 2009
- Panelist: International Symposium on Defect and Fault Tolerance in VLSI Systems (**DFT**), October 2009
- Panelist: IEEE Workshop on RTL Testing (**WRTL-T-08**), Nov. 2008, Title: Power-Aware Testing in Integrated Circuits

Podcast

1. Citi Bank, Shadman Zafar, CIO, Future Technology Trends

Special Session Organizer

- **Special Session Organizer**, Hardware Security, International Test Conference (ITC), 2018

- **Special Session**, Emerging Topics in Security and Trust I, International Test Conference (ITC), 2017 (Speakers: Brian Dupaix (AFRL), Patrick Schaumont (Virginia Tech), and An Chen (Semiconductor Research Corporation))
- **Special Session**, Emerging Topics in Security and Trust II, International Test Conference (ITC), 2017 (Domenic Forte (University of Florida), Jeyavijayan Rajendran (Texas A&M University), and Krishnendu Chakrabarty (Duke University))
- **Special Session**, Physical Attacks: Can Test Save Us? IEEE VLSI Test Symposium (VTS), 2017, Co-organized by Swarup Bhunia, University of Florida
- **Special Session 1**, IP Protection, IEEE Microprocessor Test and Verification, 2016
- **Special Session 2**, Test for Security and Trust, IEEE Microprocessor Test and Verification (MTV), 2016
- **Special Session**, Test for Security and Trust of Integrated Circuits, International Test Conference (ITC), 2016
- **Special Session**, IEEE VLSI Test Symposium (VTS), 2016, Title: Security Validation in IOT Space
- **Special Session**, IEEE VLSI Design, India, 2016, Title: New Topics in Hardware Security
- **Special Session**, IEEE Microprocessor Test and Verification Workshop (MTV), Austin, 2015, Title: New Directions in Hardware Security
- **HOT Topic Session on Counterfeit Electronics**, IEEE VLSI Test Symposium (VTS), May 2013 (with Prof. Ilia Polian, University of Passau)
- **HOT Topic Session on Smart Silicon**, IEEE VLSI Test Symposium (VTS), May 2011 (with LeRoy Windemberg, Freescale Semiconductor)
- **Moderator, Roundtable on Hardware Security and Trust**, IEEE Design & Test Magazine, September/October 2011

Panel and Tutorial Organizer/Moderator

- **Panel Organizer/Moderator**, IEEE HOST, CHIPS Act impact on Supply Chain, Onshoring, Assurance, and US Industry, May 2023
- **Panel Organizer/Moderator**, GomacTech, Quantifiable Assurance: From IPs to SoCs, March 2022
- **Panel Organizer/Moderator**, International Test Conference (ITC), Perspectives on the Future of Hardware Security, 2019
- **Panel Moderator**, Chip to PCB Assurance: Detection and Prevention, International Conference on Physical Assurance and Inspection of Electronics (PAINE), 2019.
- **Panel Organizer**, AI-Enabled Security Validation and Test, IEEE VLSI Test Symposium (VTS), 2019
- **Panel Organizer/Moderator**, Physical Inspection and Attacks: New Frontiers in Hardware Security, International Test Conference (ITC), 2018
- **Panel Organizer/Moderator**: Crossroad Between Physical Inspection and Hardware Security, IEEE International Workshop on Physical Attacks and Inspection on Electronics (PAINE), San Francisco, June 2018.
- **Tutorial Organizer**: Security of Internet of Things (IoT) and Cyber-Physical Systems (CPS): A Hands-on Approach, Design Automation Conference (DAC), 2018, Presenter: Prof. Yier Jin, University of Florida
- **Fireside Interview** with Edna Conway, CSO, Global Value Chain, Cisco
- **Tutorial Organizer**, DAC, Security of Internet of Things (IoT) and Cyber-Physical Systems (CPS): A Hands-on Approach, **Presenter**: Yier Jin, June 2018
- **Panel Organizer**, AsianHOST, Co-organized by Dr. Yousef Iskander, Technical Lead, Cisco
- **Panel Organizer**, Automotive Safety and Security: The Impending Challenges and Hopes on the Horizon, International Test Conference (ITC), 2017, Co-organized by Yervant Zorian, Vice President, Synopsys
- **Panel Organizer**, Test and Security for IoTs, International Test Conference (ITC), 2016
- **Panel Organizer**, IEEE International Verification and Security Workshop (IVSW), 2016, DFT vs. Security – Is it a Contradiction? How Can we Get the Best of Both World?

- **Panel Organizer and Moderator**, IEEE International Hardware-Oriented Security and Trust (HOST), 2016, IP Protection from Chip-to-System Using Reverse Engineering
- **Panel Organizer**, IEEE International Hardware-Oriented Security and Trust (HOST), 2016, Hardware-based System Security
- **Panel Organizer**, IEEE VLSI Test Symposium (VTS), 2016, Test Opportunities for Secure Hardware
- **Panel Organizer**, Design Automation Conference (DAC), 2013 (**Panel 1**: Advanced Node Reliability: Are we in Trouble?)
- **Panel Organizer**, Design Automation Conference (DAC), 2013 (**Panel 2**: Is Security the New Design Dimension?)
- **Panel Organizer/Moderator**, IEEE Hardware-Oriented Security and Trust (HOST), June 2012
- **Moderator**, Special Session on Smart Silicon, IEEE VLSI Test Symposium (**VTS**), May 2011
- **Panel Moderator**, Title: *Low Power Testing*, IEEE VLSI Test Symposium (**VTS**), May 2011
- **Panel Organizer**, Title: *Test and Diagnosis for Parametric Failures*, Int. Workshop on Defect and Data Driven Testing, (**D3T**), Nov. 2009
- **Panel Organizer**, Title: *Challenges in Test Data Collection and Analysis*, Int. Workshop on Defect and Data Driven Testing, (**D3T**), Oct. 2008
- **Panel Organizer**, Title: *Zero Defect (Zero DPPM): How can we get there?*, Int. Symposium on Defect and Fault Tolerance in VLSI Systems (**DFT**), Oct. 2008
- **Panel Organizer** (with Kee Sup Kim from Intel), Title: *Three Questions to Oracle (Data required for test engineers and researchers in academia)*, IEEE VLSI Test Symposium (**VTS**), 2006
- **Panel Organizer** (with Hank Walker, Texas A&M University), Title: *Process Variations + Systematic Defects: Can DBT Help?*, International Workshop on Defect-Based Testing (**DBT**), 2007.

Proposal Reviewer/Panelist

- National Science Foundation (NSF)
- Army Research Office (ARO)
- Einstein Foundation, Germany
- Hong Kong Foundation
- Sultanate Oman, Dean of Research

Membership:

- **Fellow**, ACM
- **Fellow**, IEEE
- **Fellow**, National Academy of Inventors (NAI)
- **Fellow**, AAIA
- **Fellow**, AIIA
- **Fellow**, Academy of Science, Engineering, and Medicine of Florida (ASEMFL)
- **Fellow**, Connecticut Academy of Science and Engineering (CASE)
- **Golden Core Member**, IEEE Computer Society
- **Member**, ACM SIGDA
- **Member**, TTTC
- **Member**, AAAS

Program Committee Membership

- SRC SMART JumpStart Tech and Project Description Committee, 2024
- Semiconductor Research Corporation (SRC) MAPT, 2022-2024
- International Test Conference (ITC), 2011-present
- Microprocessor Test and Verification Workshop, 2012-present
- Smart City Security and Privacy (SCSP), 2016
- ASP-DAC, 2016

- IEEE International Symposium on Computer Architecture and Digital Design (CADD), 2015
- IEEE Int. Symposium on VLSI Design and Test (VDATE), 2014-2015
- International Symposium on Research in Attacks, Intrusions and Defenses (RAID), 2017
- EDAA Outstanding Dissertation, European Design and Automation Association (EDAA), 2014-2015
- IEEE Latin American Test Workshop (LATW), 2015
- USENIX, 2014
- CSI International Symposium on Computer Architecture & Digital Systems (CADD 2017)
- Design Automation Conference (DAC), 2011-2014, 2017
- International Symposium on Quality Electronic Design (ISQED), 2014
- TRUDEVICE Workshop on Test and Fault Tolerance for Secure Devices, 2014
- Design Automation Conference (DAC) Panel Committee, 2013
- IEEE Conference on Very Large Scale Integration (VLSI-SoC), 2012-present
- IEEE CS Annual Symposium on VLSI (ISVLSI), 2012-present
- International Test Conference (ITC)-Asia, 2017-present
- Design, Automation, and Test in Europe (DATE), 2009-2010, 2013, 2016-present
- European Test Symposium (ETS), 2010-present
- IEEE VLSI Test Symposium (VTS), 2009-present
- ACM SIGDA PhD DAC Forum, 2008-2011, 2015
- IEEE Workshop on RTL and High Level Testing (WRTLTL), 2009-2011
- ACM Great Lake Symposium on VLSI (GLSVLSI), 2008-present
- International Conf. on Communication Theory, Reliability, and Quality of Service (CTRQ), 2008-2013
- IEEE Int. Workshop on Defect Based Testing (DBT), 2005-2010
- Int. Conference on Computer Design (ICCD), 2008-present
- North Atlantic Test Workshop (NATW) 2004-present
- IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems (DFT), 2005-present
- International Design and Test Workshop (IDT), 2006-present
- International Symposium on Nanoscale Architectures (NanoArch), 2007-2010
- IEEE Int. On-Line Testing Symposium (IOLTS), 2009
- Int. Workshop on Impact of Low-Power Design on Test and Reliability, 2009-present
- Workshop on Unique Chips and Systems (UCAS), 2009
- IEEE Workshop on Design for Reliability and Variability (DRV), 2009

Session Chair

- International Test Conference (ITC), 2015
- Design Automation Conference, 2015
- DMSMS, 2013
- International Test Conference (ITC), 2013
- Design Automation Conference (DAC), 2012
- Int. Workshop on Current and Defect-Based Testing (DBT), 2005
- Int. Workshop on Current and Defect-Based Testing (DBT'), 2005
- IEEE North Atlantic Test Workshop (NATW), 2006, 2007, 2008, 2009
- International Symposium on Defect and Fault Tolerance in VLSI Systems (DFT), 2006
- Design Automation Conference (DAC), 2007
- International Symposium on Nanoscale Architectures (NanoArch), 2008
- International Test Conference (ITC), 2006, 2008, 2009
- IEEE Workshop on RTL and High Level Testing (WRTLTL), 2008
- IEEE VLSI Test Symposium (VTS), 2010
- International Test Conference (ITC), 2013

Session Coordinator

- International Test Conference (ITC), 2011

Training

- MEST Center Training on Hardware Security, 2020 (9 hour teaching)

External Committee Membership

- NDIA Systems Security Engineering Committee

Additional Activities

- Robust Design Program (<http://www.robust-designs.com/>)
- Journal of Electronic Testing: Theory and Applications (JETTA) Best Paper Review Committee, 2018

Review Activity

- National Science Foundation (NSF)
- Army Research Office (ARO)
- Oman, Sultan Ghaboos University Foundation, Dean of Research
- IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)
- IEEE Transactions on Very Large Scale Integration Systems (TVLSI)
- IEEE Transactions on Computers
- ACM Journal on Emerging Technologies in Computing Systems (JETC)
- ACM Transactions on Design Automation of Electronic Devices (TODAES)
- International Journal of Computers and Applications
- IEEE Circuits, Devices & Systems
- IEEE Design & Test of Computers Magazine
- Journal of Low Power Electronics (JOLPE)
- IBM Journal of Research and Developments
- IEEE Communication Magazine
- IEEE International Test Conference (ITC)
- IEEE VLSI Test Symposium (VTS)
- IEEE Asian Test Symposium (ATS)
- IEEE North Atlantic Test Workshop (NATW)
- IEEE Workshop on Defect-Based Testing (DBT)
- IEEE International Conference on Microelectronics (ICM)
- Design Automation Conference (DAC)
- IEEE Symp. on Defect and Fault Tolerance in VLSI Systems (DFT)
- Great Lake Symposium on VLSI (GLS-VLSI)

Publications (Citation: 27,5000 , H-index: 85)

Books

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- Pre-Silicon Electromagnetic Fault Injection Security Evaluation for Robust IC Design,”** IEEE Int. Symposium on Hardware-Oriented Security and Trust (HOST), 2025.
12. A. M. Shuvo, L. Rahman, J. Zhou, F. Farahmandi and M. Tehranipour, “**A System-Aware Remote Fault-Injection Attack Detection & Mitigation for Secure Heterogeneous Systems,**” IEEE Int. Symposium on Hardware-Oriented Security and Trust (HOST), 2025 (**Best Paper Award**).
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 22. A. Uddin, S. K. Saha, F. Farahmandi, and M. Tehranipour, “**Case Study: Fault-Injection Vulnerability Assessment at RTL Level,**” IEEE Physical Assurance and Inspection of Electronics (PAINE), 2024.
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 24. S. Islam, S. Khan, F. Farahmandi, M. Tehranipour, and N. Asadi, “**CAKE-SiP: Chiplet Authenticate & Key Exchange for Secure Provisioning in System-in-Package,**” IEEE Physical Assurance and Inspection of Electronics (PAINE), 2024 (**Best Poster Candidate**).
 25. G. Haidar, S. Islam, J. Zhou, K. Z. Azar, M. Tehranipour, and F. Farahmandi, “**SECT-HI: Enabling Secure Testing for Heterogeneous Integration to Prevent SiP Counterfeits,**” International Test Conference (ITC), 2024.
 26. B. Ahmed, J. Zhou, S. Saha, S. Aftabjahani, M. Tehranipour, and F. Farahmandi, “**Continuity in Security: Leveraging LLM for Translating Security Properties Across Hardware Designs,**” Int. Conference on Very Large-Scale Integration (VLSI-SoC), 2024 (**Best Paper Candidate**).
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36. G. I. Haidar, K. Z. Azar, H. M. Kamali, M. Tehranipoor, and F. Farahmandi, **"GATE-SiP: Enabling Authenticated Encryption Testing in Systems-in-Package,"** Design Automation Conference (DAC), 2024.
37. H. Li, L. Lin, N. Chang, S. Chowdhury, M. Tehranipoor, K. Monta, and M. Nagata, **"ML-Based Optimal Virtual Placement Exploration for EM Side-Channel Mitigation"** DesignCon, 2024 (Best Paper Candidate).
38. M. Sami, K. Azar, H. Kamali, F. Farahmandi, and M. Tehranipoor, **"PQC-HIL PQC-enabled Chiplet authentication and Key Exchange in Heterogeneous Integration,"** Electronics Components and Technology (ECTC), 2024.
39. N. Mondol, A. Vafaei, K. Z. Azar, F. Farahmandi, and M. Tehranipoor, **"RL-TPG: Automated Pre-silicon Security Verification through Reinforcement Learning-based Test Pattern Generation,"** Design Automation and Test in Europe (DATE), 2024.
40. S. R. Rajendran, F. Farahmandi, and M. Tehranipoor, **"CAD Tools Pathways in Hardware Security,"** International Conference on VLSI Design (VLSID), 2024.
41. N. F. Dipu, M. M. Hossain, K. Z. Azar, F. Farahmandi, and M. Tehranipoor, **"FormalFuzzer: Formal Verification Assisted Fuzz Testing for SoC Vulnerability Detection,"** Asian and South Pacific Conference on Design Automation Conference (ASP-DAC), 2024.
42. M. R. Muttaki, H. M. Kamali, M. Tehranipoor and F. Farahmandi, **"PALLET: Protecting Analog Devices using a Last-Level Edit Technique,"** IEEE Conference on Physical Assurance and inspection of Electronics (PAINE), 2023.
43. M. S. Ul Haque, R. Guo, M. Sazadur Rahman, H. M. Kamali, F. Farahmandi and M. Tehranipoor, **"SHI-Lock: Enabling Co-Obfuscation for Secure Heterogeneous Integration against RE and Cloning,"** IEEE Conference on Physical Assurance and inspection of Electronics (PAINE), 2023.
44. M. Hossain, N. D. Farzana, K. Z. Azar, F. Rahman, and M. Tehranipoor, **"TaintFuzzer: SoC Security Verification using Taint Inference-enabled Fuzzing,"** Int. Conference on Computer-Aided Design (ICCAD), 2023.
45. R. Kibria, F. Farahmandi and M. Tehranipoor, **"ARC-FSM-G: Automatic Security Rule Checking for Finite State Machine at the Netlist Abstraction,"** International Test Conference (ITC), 2023. Best Paper Candidate and Honorable mention Award

46. P. P. Sarker, U. Das, M. Monjil, H. M. Kamali, F. Farahmandi, and Mark Tehranipoor, "**GEM-Water: Generation of EM-based Watermark for SoC IP Validation with Hidden FSMs,**" International Symposium for Testing and Failure Analysis (ISTFA), 2023.
47. S. Rahman, N. Varshney, F. Farahmandi, N. Asadi, and M. Tehranipoor, "**LLE: Mitigating IC Piracy and Reverse Engineering by Last Level Edit,**" International Symposium for Testing and Failure Analysis (ISTFA), 2023.
48. H. Al-Shaikh, M. B. Monjil, K. Z. Azar, F. Farahmandi, M. Tehranipoor, and F. Rahman, "**QuardTropy: Detecting and Quantifying Unauthorized Information Leakage in Hardware Designs using g-entropy,**" IEEE Defect and Fault Tolerant Systems (DFTS), 2023.
49. M. Monir, K. Z. Azar, F. Farahmandi, and M. Tehranipoor, "**EmuFuzzer: Emulation-based Cost Function Guided Fuzzing for SoC Vulnerability Detection,**" SRC TECHCON, 2023.
50. S. Tarek, S. Rajendran, M. Tehranipoor, and F. Farahmandi, "**Benchmarking of SoC-level Hardware Vulnerabilities: A Complete Walkthrough,**" ISVLSI, 2023.
51. D. Volya, T. Zhang, N. Alam, M. Tehranipoor, and O. Mishra, "**Towards Secure Classical-Quantum Systems,**" IEEE International Symposium on Hardware-Oriented Security and Trust (HOST), 2023.
52. Y. Bai, J. Park, M. Tehranipoor, and D. Forte, "**Dual Channel EM/Power Attack Using Mutual Information and its Real-time Implementation,**" IEEE International Symposium on Hardware-Oriented Security and Trust (HOST), 2023.
53. T. Rahman, K. Bepary, S. Haque, M. Tehranipoor, and F. Rahman, "**Design and Security Mitigation of Configurable and Generative Hardware Cryprosystems,**" IEEE Dallas Circuits and Systems (DCAS) Conference, 2023.
54. Z. Ibnat, S. Rahman, M. Tehranipoor, and F. Farahmandi, "**ActiWate: Adaptive Design-agnostic Active Watermark for IP Ownership in Modern SoCs,**" Design Automation Conference (DAC), 2023.
55. U. Das, M. S. Rahman, N. N. Anandakumar, K. Zamiri Azar, F. Rahman, M. Tehranipoor, and Farimah Farahmandi, "**PSC-Watermark: Power Side Channel Based IP Watermarking Using Clock Gates,**" IEEE European Test Symposium (ETS), 2023.
56. T. Zhang, M. Tehranipoor, and F. Farahmandi, "**BitFREE: On Significant Speedup and Security Applications of FPGA Bitstream Format Reverse Engineering,**" IEEE European Test Symposium (ETS), 2023.
57. B. Ahmed, M. Tehranipoor, and F. Farahmandi, "**SoC Security Verification: Challenges and Solutions,**" IEEE VLSI Test Symposium (VTS), 2023.
58. M. M. Rahman, S. M. Rahman, R. Kibria, M. Borza, B. Reddy, A. Cron, F. Rahman, M. Tehranipoor, and F. Farahmandi, "**CAPEC: A Cellular Automata Guided FSM-based IP Authentication Scheme,**" IEEE VLSI Test Symposium (VTS), 2023.
59. T. Zhang, L. Rahman, H. M. Kamali, K. Z. Azar, M. Tehranipoor, and F. Farahmandi, "**Fault Injection Detection in Secure Heterogeneous Integration via Power Noise Variations,**" Electronic Components and Technology Conference (ECTC), 2023.
60. M. R. Muttaki, S. Saha, H. M. Kamali, F. Rahman, M. Tehranipoor and F. Farahmandi, "**RTLlock: IP Protection using Scan-Aware Logic Locking at RTL,**" Design Automation and Test in Europe (DATE), 2023. **Nominated for Best Paper Award.**
61. S. R. Rajendran, S. Tarek, B. M. Hicks, H. M. Kamali, F. Farahmandi and M. Tehranipoor, "**HUnTer: Hardware Underneath Trigger for Exploiting SoC-level Vulnerabilities,**" Design Automation and Test in Europe (DATE), 2023.
62. R. Guo, M. S. Rahman, H. M. Kamali, F. Rahman, F. Farahmandi and M. Tehranipoor, "**EvoLUTe: Evaluation of Look-Up-Table-based Fine-Grained IP Redaction,**" Design Automation and Test in Europe (DATE), 2023. **Nominated for Best Paper Award.**
63. H. M. Kamali, K. Z. Azar, F. Farahmandi and M. Tehranipoor, "**SheLL: Shrinking eFPGA Fabrics for Logic Locking,**" Design Automation and Test in Europe (DATE), 2023.
64. M. M. Hossain, A. Vafaei, K. Z. Azar, F. Rahman, F. Farahmandi and M. Tehranipoor, "**SoCFuzzer: SoC Vulnerability Detection using Cost Function enabled Fuzz Testing,**" Design Automation and Test in Europe (DATE), 2023. **Nominated for Best Paper Award.**

65. M. S. Haque, F. Rahman, F. Farahmandi, and M. Tehranipoor, “**Countering Reverse Engineering and Cloning in Heterogeneously Integrated Systems**,” GomacTech, 2023.
66. J. Harrison, Nathan Jessurun, N. Asadi, and M. Tehranipoor, “**Exploration of Automated Laser Marking Analysis for Counterfeit IC Identification**,” GomacTech, 2023.
67. M. K. Bepray, F. Rahman, F. Farahmandi, and M. Tehranipoor, “**Security Assessment and Modeling of EM Side-Channel Leakage at Gate-Level**,” GomacTech, 2023.
68. E. Tawfik, et. al. “**Holistic Secure SoC Design for Resource Constrained Applications**,” GomacTech, 2023.
69. M. Monjil, F. Rahman, F. Farahmandi, and M. Tehranipoor, “**Robust Verification for Physical Inspection Based Chiplet Authentication**,” GomacTech, 2023.
70. S. R. Rajendran, M. Tehranipoor, and F. Farahmandi, “**An ISA-based Software Snippet Generation for Exploiting Hardware Vulnerabilities**,” GomacTech, 2023.
71. S. Shi, N. Pundir, H. Mardani Kamali, M. Tehranipoor, F. Farahmandi, “**SecHLS: Enabling Security Awareness in High-Level Synthesis**,” Asian and South Pacific Conference on Design Automation Conference (ASP-DAC), 2023.
72. H. Al-Shaikh, A. Vafaei, M. Md Mashahedur Rahman, K. Zamiri Azar, F. Rahman, F. Farahmandi, M. Tehranipoor, “**SHarPen: SoC Security Verification by Hardware Penetration Test**,” Asian and South Pacific Conference on Design Automation Conference (ASP-DAC), 2023.
73. R. Muttaki, M. Tehranipoor, and F. Farahmandi, “**FTC: A Universal Low-Overhead Fault-Injection Attack Detection Solution**,” International Symposium for Testing and Failure Analysis (ISTFA), 2022.
74. N. Pundir, H. Li, L. Lin, N. Chang, “**SPILI: Security Properties and Machine Learning Assisted Pre-silicon Laser Fault Injection Assessment**,” International Symposium for Testing and Failure Analysis (ISTFA), 2022.
75. R. Kibria, S. Rahman, F. Farahmandi, and M. Tehranipoor, “**RTL-FSMx: Fast and Accurate Finite State Machine Extraction at the RTL for Security Application**,” International Test Conference (ITC), 2022.
76. U. Das, R. Muttaki, m. Tehranipoor, and F. Farahmandi, “**ADWIL: A Zero-Overhead Analog Device Watermarking Using Inherent IP Features**,” International Test Conference (ITC), 2022.
77. A. Mazumder Shuvo, N. Pundir, J. Park, F. Farahmandi, and M. Tehranipoor, “**LDTFI: Layout-Aware Timing Fault-Injection Attack Assessment Against Differential Fault Analysis**,” IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 2022.
78. N. Jessurun, J. Harrison, M. Tehranipoor, and N. Asadi, “**PinPoint: An SMD Pin Localization Method**” IEEE International Symposium on Physical and Failure Analysis (IPFA), 2022.
79. K. Zamiri Azar, H. Kamali, F. Farahmandi, and M. Tehranipoor, “**Warm Up before Circuit De-obfuscation? An Exploration of Possibilities**,” IEEE International Symposium on Hardware-Oriented Security and Trust (HOST), 2022.
80. R. Muttaki, M. Tehranipoor, and F. Farahmandi, “**FTC: A Universal Fault Injection Attack Detection Sensor**,” IEEE International Symposium on Hardware-Oriented Security and Trust (HOST), 2022.
81. N. Pundir, L. Lin, N. Chang, F. Farahmandi, and M. Tehranipoor, “**Security Property Driven Pre-Silicon Laser Fault Injection Assessment**,” IEEE International Symposium on Hardware-Oriented Security and Trust (HOST), 2022.
82. S. Rahman, R. Guo, H. M. Kamali, M. Abdel-Moneum, F. Farahmandi, F. Rahman, and M. Tehranipoor, “**O’Clock: Lock the Clock via Clock-gating for SoC IP Protection**,” Design Automation Conference (DAC), 2022.
83. R. Kibira, N. Farzana, F. Farahmandi, and M. Tehranipoor, “**FSMx: Finite State Machine Extraction from Flattened Netlist with Application to Security**,” IEEE VLSI Test Symposium (VTS), 2022.
84. C. Xi, N. Jessurun, A. Khan, M. Tehranipoor, and N. Asadi, “**A Naturally Inherent Tracking Methodology for Secure Packaging Using Geo-Magnetic Signatures**,” GomacTech, 2022.
85. P. Calzada, J. Harrison, P. Chawla, N. Asadi, and M. Tehranipoor, “**PCB Trojan Detection using Optical Imaging**,” GOMACTech, 2022.

86. M. Farmani, J. Harrison, F. Rahman, and M. Tehranipoor, "**Efficient Rowhammer-Aware DRAM Test Under Reduced Voltage and Increased Temperature**," GOMACTech, 2022.
87. M. Azhagan, M. Y. Vutukuru, O. Paradis, M. Tehranipoor, N. Asadi, "**Logo Detection and Localization for IC Authentication, Marking Recognition, and Counterfeit Detection**," GOMACTech, 2022.
88. N. Vashishta, Al Hassan, Md. Mahfuz, F. Rahman, N. Asadi, and M. Tehranipoor, "**Trust Validation of Chiplets using a Physical Inspection Based Certificate Authority**," Electronic Components and Technology Conference (ECTC), 2022.
89. D. Mehta, N. Mondol, F. Farahmandi, and M. Tehranipoor, "**AIME: Watermarking AL Models by Leveraging Errors**," Design, Automation, and Test in Europe (DATE), 2022.
90. T. Zhang, F. Rahman, M. Tehranipoor, and F. Farahmandi, "**FPGA-Chain: Enabling Holistic Protection of FPGA Supply Chain with Blockchain Technology**," IEEE Workshop on Silicon Lifecycle Management (SLM), Oct. 2021.
91. H. Wang, H. Li, F. Rahman, F. Farahmandi, and M. Tehranipoor, "**Security Property-Driven Fault-Injection Vulnerability Assessment of Modern SoCs**," iSecCon, 2021.
92. S. U. Sami, F. Rahman, D. Donchin, A. Cron, M. Borza, F. Farahmandi, and M. Tehranipoor, "**POCA: First Power-on Chip Authentication in Untrusted Foundry and Assembly**," IEEE International Symposium on Hardware-Oriented Security and Trust (HOST), 2021.
93. S. Rahman, H. Li, R. Guo, F. Rahman, F. Farahmandi, and M. Tehranipoor, "**LL-ATPG: Logic-Locking Aware Test Using Valet Keys in an Untrusted Environment**," International Test Conference (ITC), 2021.
94. A. Vafaei, N. Hooten, M. Tehranipoor, and F. Farahmandi, "**Symba: Symbolic Execution at C-level for Hardware Trojan Detection**," International Test Conference (ITC), 2021.
95. B. Ahmed, F. Rahman, N. Hooten, F. Farahmandi, and M. Tehranipoor, "**AutoMap: Automated Mapping of Security Properties Between Different Levels of Abstraction in Design Flow**," International Conference on Computer-Aided Design (ICCAD), 2021.
96. N. Pundir, S. Shi, M. Tehranipoor, and F. Farahmandi, "**HLS-Induced Information Leakage Verification**," SRC TECHCON, 2021.
97. J. True, N. Jessurun, D. Mehta, M. Tehranipoor, N. Asadizanjani, "**Q.U.A.I.N.T.P.E.A.X. QUantifying Algorithmically INtrinsic Properties of Electronic Assemblies via X-ray CT**", Microscopy and Microanalysis (M&M), August 2021.
98. J. True, C. Xi, N. Jessurun, K. Ahi, M. Tehranipoor, N. Asadizanjani, "**Terahertz Based Machine Learning Approach to Integrated Circuit Assurance**" Electronic Components and Technology Conference (ECTC), June 2021
99. M. M. Al Hasan, N. Vashishta, S. Taheri, M. Tehranipoor, N. Asadizanjani "**Generative Adversarial Network for Integrated Circuits Physical Assurance Using Scanning Electron Microscopy**", IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA), September 2021.
100. M. M. Rahman, S. Mohammad, J. Vosatka, J. Allen, M. Allen, F. Farahmandi, F. Rahman, and M. Tehranipoor, "**HEXON: Protecting Firmware Using Hardware-Assisted Execution-Level Obfuscation**," International Symposium on VLSI (ISVLSI), 2021.
101. T. Farheen, U. Boreto, N. Varshney, H. Shen, D. Woodard, M. Tehranipoor, and D. Forte, "**Proof of Reverse Engineering Barrier: SEM Image Analysis on Covert Gates**," International Symposium on Test and Failure Analysis (ISTFA), 2021.
102. S. Aftabjahani, R. Kastner, M. Tehranipoor, F. Farahmandi, J. Oberg, A. Nordstrom, N. Fern, A. Alric, "**CAD for Hardware Security – Automation is Key to Adoption of Solution**," IEEE VLSI Test Symposium (VTS), 2021.
103. H. Wang, F. Farahmandi, and M. Tehranipoor, "**SoFI: Security Property-Driven Vulnerability Assessment of ICs Against Fault-Injection Attacks**," SNUG, 2021.
104. Md. S. Ul Islam, F. Rahman, Farimah Farahmandi, A. Cron, M. Borza, and Mark Tehranipoor, "**End-to-End Secure SoC Lifecycle Management**," Design Automation Conference (DAC), 2021.

105. T. Zhang, J. Park, M. Tehranipoor, and F. Farahmandi, "**PSC-TG: RTL Power Side-Channel Leakage Assessment with Test Pattern Generation**," Design Automation Conference (DAC), 2021.
106. R. Muttaki, M. Tehranipoor, and F. Farahmandi, "**HLock: Locking IPs at the High-Level Language**," Design Automation Conference (DAC), 2021.
107. M. Farmani, F. Rahman, and M. Tehranipoor, "**RHAT: Efficient RowHammer-Aware Test for Modern DRAM Modules**," IEEE European Test Symposium (ETS), 2021.
108. N. Dipu, A. Ayalasomayajula, F. Rahman, F. Farahmandi, and M. Tehranipoor, "**SAIF: Automated Asset Identification for Security Verification at the Register Transfer Level**," IEEE VLSI Test Symposium (VTS), 2021.
109. J. Harrison, P. Calzada, N. Asadi, and Mark Tehranipoor, "**A Comprehensive Benchmark Suite for PCB Assurance**," GoamcTech 2021.
110. A. Khan, C. Xi, N. Asadi, and Mark Tehranipoor, "**Security Assessment of Interposer in Advanced Packaging**," GomacTech 2021.
111. H. Wang, H. Li, F. Farahmandi, and Mark Tehranipoor, "**SOFI: Security Property-Driven Vulnerability Assessment of ICs Against Fault-Injection Attacks**," GoamcTech 2021.
112. O. Paradis, D. Woodard, M. Tehranipoor, and N. Asadi, "**Frameowrk for Automatic OCB Marking Detection and Recognition for Hardware Assurance**," GOMACTech 2021.
113. N. Jessurun, O. Paradis, M. Tehranipoor, N. Asadi, "**Improvements on the SHADE Algorithm for PCB Component Estimate Refinement**," GOMACTech 2021.
114. N. Pundir, F. Farahmandi, and M. Tehranipoor, "**Secure High-Level Synthesis: Challenges and Solutions**," International Symposium on Quality Electronics Design (ISQED), 2021.
115. M. M. Hossain, F. Farahmandi, M. Tehranipoor and F. Rahman, "**BOFT: Exploitable Buffer Overflow Detection by Information Flow Tracking**," Design, Automation, and Test in Europe (DATE), 2021.
116. O. Paradis, N. Jessurun, M. Tehranipoor, and N. Asadi, "**Color Normalization for Robust Automatic Bill of Materials Generation and Visual Inspection of PCBs**," International Symposium on Test and Failure Analysis (ISTFA), 2020.
117. L. Lavdas, M. T. Rahman, M. Tehranipoor, and N. Asadi, "**On Optical Attacks Making Logic Obfuscation Fragile**," International Test Conference, Asia (ITC-Asia), 2020.
118. A. Stern, D. Mehta, S. Tajik, F. Farahmandi, and M. Tehranipoor, "**SPARTA: A Laser Probing Approach for Trojan Detection**," International Test Conference (ITC), 2020.
119. A. Stern, D. Mehta, S. Tajik, U. Guin, F. Farahmandi, and M. Tehranipoor, "**Trust Assessment for Electronic Components using Laster and Emission-based Microscopy**," IEEE RAPID, 2020.
120. J. Vosatka, A. Stern, M. Hossain, F. Rahman, J. Allen, M. Allen, F. Farahmandi, and M. Tehranipoor, "**Confidence Modeling and Tracking of Recycled Integrated Circuits, Enabled by Blockchain**," IEEE RAPID, 2020.
121. H. Lu, N. Vashishta, N. Asadi, M. Tehranipoor, D. Woodard, "**Knowledge-based Object Localization in Scanning Electron Microscopy Images for Hardware Assurance**," International Symposium on Test and Failure Analysis (ISTFA), 2020.
122. O. Paradis, N. Jessurun, M. Tehranipoor, and N. Asadi, "**Color Normalization for Robust Automatic Bill of Materials Generation and Visual Inspection of PCBs**," International Symposium on Test and Failure Analysis (ISTFA), 2020.
123. N. Jessurun, O. Paradis, M. Tehranipoor, and N. Asadi, "**SHADE: Automated Refinement of PCB Component Estimates Using Detected Shadows**," IEEE Conference on Physical Assurance and Inspection of Electronics (PAINE), 2020. **Received Best Student Paper Award**
124. J. Vosatka, A. Stern, M. M. Hossain, F. Rahman, F. Allen, M. Allen, F. Farahmandi, and M. Tehranipoor, "**Tracking Cloned Elecronic Components using a Consortium-based Blockchain Infrastructure**," IEEE Conference on Physical Assurance and Inspection of Electronics (PAINE), 2020.
125. A. Stern, D. Mehta, S. Tajik, U. Guin, F. Farahmandi, and M. Tehranipoor, "**SPARTA: Laser Probing Approach for Sequential Trojan Detection in COTS Integrated Circuits**," IEEE Conference on Physical Assurance and Inspection of Electronics (PAINE), 2020.

126. A. Duncan, A. Nahiyani, F. Rahman, G. Skipper, M. Swamy, A. Lukefahr, F. Farahmandi, and M. Tehranipoor, "**SERFI: Secure Remote FPGA Initialization in an Untrusted Environment**," IEEE VLSI Test Symposium (VTS), 2020.
127. N. Pundir, F. Rahman, M. Tehranipoor, and F. Farahmandi, "**Analyzing Security Vulnerabilities Induced by High-Level Synthesis**," GomacTech 2020.
128. J. Vosatka, M.M. Hossain, F. Rahman, J. Allen, M. Allen, F. Farahmandi, and M. Tehranipoor, "**Modeling Risk in Electronics Supply Chains Enabled by Blockchain**," GomacTech 2020.
129. A. Stern, A. Duncan, S. Tajik, F. Farahmandi, and M. Tehranipoor, "**Sequential Hardware Trojan Detection using Clock Activity Analysis**," GomacTech, 2020.
130. A. Duncan, A. Nahiyani, F. Rahman, G. Skipper, M. Swamy, A. Lukefahr, F. Farahmandi, and M. Tehranipoor, "**SERFI: Secure Remote FPGA Initialization**," GomacTech, 2020.
131. T. Rahman, S. M. Rahman, S. Tajik, M. Tehranipoor, and N. Asadi, "**The Key is Left Under the Mat: On the Inappropriate Security Assumption of Logic Locking Schemes**," IEEE International Hardware-Oriented Security and Trust (HOST), 2020.
132. M. Azhagan, M. D. Mehta, H. Lu, S. Agrawal, M. Tehranipoor, D. Woodard, N. Asadizanjani, "**A Review on Automatic Bill of Material Generation and Visual Inspection on PCBs**," International Symposium for Testing and Failure Analysis (ISTFA), Portland, NV, 2019.
133. D. Forte, S. Bhunia, Ramesh Karri, J. Plusquellic, and M. Tehranipoor, "**IEEE International Hardware-Oriented Security and Trust (HOST): Past, Present, and Future**" International Test Conference (ITC), 2019.
134. N. Farzana, F. Rahman, M. Tehranipoor, and F. Farahmandi, "**Security Verification of System on Chip using Property Checking**," International Test Conference (ITC), 2019.
135. A. Duncan, F. Rahman, A. Lukefahr, F. Farahmandi, and M. Tehranipoor, "**FPGA Bitstream Security: A Day in the Life**," International Test Conference (ITC), 2019.
136. M. Azhagan, D. Mehta, H. Lu, S. Agrawal, P. Chawla, M. Tehranipoor, D. Woodard, and Navid Asadi, "**A New Framework for Automated Bill of Material Generation and Visual Inspection**," International Symposium on Test and Failure Analysis (ISTFA), 2019.
137. M. Alam, F. Ganji, S. Tajik, M. Tehranipoor, and D. Forte, "**RAM-Jam: Remote Temperature and Voltage Fault Attack on FPGAs using Memory Collisions**," Fault Diagnosis and Tolerance in Cryptography (FDTC), 2019.
138. F. Ganji, S. Tajik, J. P. Seifert, M. Tehranipoor, and D. Forte, "**Approaches for Hardness Amplification of PUFs**," PROOFS, 2019.
139. J. Park, S. Cho, T. Lim, S. Bhunia, M. Tehranipoor, "**SCR-QRNG: Side-Channel Resistant Design using Quantum Random Number Generator**," International Conference on Computer-Aided Design (ICCAD), 2019.
140. T. Aravin, H. Shen, M. Tehranipoor, and Q. Qu, "**LPN-based Device Authentication Using Resistive Memory**," ACM GLS-VLSI, 2019.
141. A. Duncan, A. Skipper, A. Stern, F. Rahman, A. Nahiyani, A. Lukefahr, M. Swamy, and M. Tehranipoor, "**FLATS: Filling Logic and Testing Spatially for FPGA Authentication and Tamper Detection**," IEEE International Hardware-Oriented Security and Trust (HOST), 2019.
142. X. Guo, M. Tehranipoor, and Y. Jin, "**QIF-Verilog: Quantitative Information-Flow based Hardware Description Languages for Pre-Silicon Security Assessment**," IEEE International Hardware-Oriented Security and Trust (HOST), 2019.
143. B. Park, M. Tehranipoor, D. Forte, and N. Maghari, "**A Metal-Via Resistance Based Physically Unclonable Function with 1.18% Native Instability**," IEEE Custom Integrated Circuits Conference (CICC), 2019.
144. J. Park, T. Miao, A. Nahiyani, A. Vassilev, Y. Jin, and M. Tehranipoor, "**RTL-PSC: Automated Power Side-Channel Leakage Assessment at Register-Transfer Level**," IEEE VLSI Test Symposium (VTS), 2019.
145. A. Stern, K. Yang, J. Vosatka, A. Duncan, J. Park, D. Forte, and M. Tehranipoor, "**RASC: Enabling Remote Access to Side-Channels for Mission Critical Systems**," GomacTech, 2019.

146. A. Duncan, A. Lukefahr, A. Stern, M. Tehranipoor, and M. Swamy, "**Lifetime Physical Authentication of FPGAs Through Infrared Watermarking**," GomacTech, 2019.
147. Q. Shi, H. Wang, N. Asadi, M. Tehranipoor, and D. Forte, "**A Comprehensive Analysis on Vulnerability of Active Shields to Tilted Microprobing Attacks**," IEEE Asian HOST (2018).
148. M. T. Rahman, Q. Shi, S. Tajik, H. Shen, D. Woodard, M. Tehranipoor, and N. Asadi, "**Physical Inspection and Attacks: New Frontier in Hardware Security**," IEEE International Verification and Security Workshop (IVSW), 2018.
149. A. Stern, U. Botero, B. Shakya, H. Shen, and M. Tehranipoor, "**EMFORCED: EM-based Fingerprinting Framework for Counterfeit Detection with Demonstration on Remarkable ICs**," International Test Conference (ITC), 2018.
150. Y. Han, X. Wang, and M. Tehranipoor, "**CIPA: Concurrent IC and PCB Authentication Using On-Chip Ring Oscillator Array**," IEEE Asian Test Symposium (ATS), 2018.
151. H. Shen, N. Asadi, M. Tehranipoor, and D. Forte, "**Nanopyramid: An Optical Scrambler Against Backside Probing Attacks**," International Symposium on Test and Failure Analysis (ISTFA), 2018.
152. H. Shen, M. Tehranipoor, and S. Bhunia, "**Tampering, Snooping, and Electromagnetic Attack Proof Coating on Printed Circuit Boards**," International Symposium on Test and Failure Analysis (ISTFA), 2018.
153. N. Vashistha, H. Shen, T. Rahman, D. Woodard, N. Asadi, and M. Tehranipoor, "**Trojan Scanner: Detecting Hardware Trojans with Rapid Imaging Combined with Image Processing and Machine Learning**," International Symposium on Test and Failure Analysis (ISTFA), 2018.
154. H. Wang, Q. Shi, D. Forte, and M. Tehranipoor, "**Metrics and Physical Design Flow for Internal Shielding Against Front Side Probing Attack**," SRC TECHCON, 2018.
155. A. Nahiyani, D. Forte, and M. Tehranipoor, "**Framework for Automated and Systematic Security Assessment of Modern SoCs**," SRC TECHCON, 2018.
156. K. Yang, J. Park, M. Tehranipoor, and S. Bhunia, "**Robust Timing Attack Countermeasure on Virtual Hardware**," IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 2018.
157. J. Park, X. Xu, Y. Jin, D. Forte, and M. Tehranipoor, "**Power-based Side-channel Instruction-level Disassembler**," Design Automation Conference (DAC), 2018.
158. M. Alam, S. Chowdhury, M. Tehranipoor, and U. Guin, "**Robust, Low-Cost, and Accurate Detection of Recycled ICs using Digital Signatures**," IEEE International Symposium on Hardware Oriented Security and Trust (HOST), 2018.
159. K. Yang, J. Park, M. Tehranipoor, and S. Bhunia, "**Hardware Virtualization for Protection against Power Analysis Attack**," IEEE International Symposium on Hardware-Oriented Security and Trust (HOST), 2018.
160. O. Arias, F. Rahman, M. Tehranipoor, and Y. Jin, "**Device Attestation: Past, Present, and Future**," Design Automation, and Test in Europe (DATE), 2018.
161. E. Principe, N. Asadi, D. Forte, M. Tehranipoor, R. Chivas, M. DiBattista, S. Silverman, M. Marsh, N. Piche, J. Mastovich, "**Steps Toward Computational Guided Deprocessing of Integrated Circuits**," GomacTech, 2018.
162. D. Capecci, G. Contreras, D. Forte, M. Tehranipoor, and S. Bhunia, "**Automated SoC Security from Design to Fabrication**," GomacTech, 2018.
163. S. Beireddy, N. Asadi, M. Tehranipoor, D. Woodard, and D. Forte, "**Automated Detection of Counterfeit IC Defects Using Image Processing**," GomacTech, 2018 (poster).
164. J. He, X. Guo, M. Tehranipoor, and Y. Jin, "**Golden Chip Free Electromagnetic Simulation and Statistical Analysis for Hardware Security**," GomacTech, 2018 (poster).
165. U. Botero, M. Tehranipoor, and D. Forte, "**Downgrade: A Framework for Obsolescence Handling through Backwards Compatibility**," GomacTech, 2018.
166. F. Rahman, M. Farmani, M. Tehranipoor, and Y. Jin, "**Hardware-assisted Cybersecurity for IoT Devices**," IEEE Microprocessor Test, Security, and Verification (MTV), 2017.

167. X. Wang, L. Yu, F. Rahman, and M. Tehranipoor, "**IV-PUF: Interconnect Variations PUF with Self-Masking Circuit for Performance Enhancement**," IEEE Microprocessor Test and Security Conference (MTV), 2017
168. S. Choudhury, X. Xu, M. Tehranipoor, and D. Forte, "**Aging-Resistant RO PUF with Increased Reliability in FPGA**," Int. Conference on Reconfigurable Computing and FPGAs (Reconfig), 2017.
169. A. Chhotaray, A. Nahiyani, T. Shrimpton, D. Forte, and Mark Tehranipoor, "**Standardizing Bad Cryptographic Practice - A teardown of the IEEE standard for protecting electronic-design intellectual property**," ACM Conference on Computer and Communication Security (CCS), 2017.
170. X. Wang, Y. Guo, T. Rahman, D. Zhang, and M. Tehranipoor, "**DOST: Dynamically Obfuscated Wrapper for Split Test against IC Piracy**," IEEE Asian Hardware-Oriented Security and Trust Symposium (AsianHOST), 2017. **Received Best Paper Award.**
171. Z. Guo, X. Xu, M. Tehranipoor, and D. Forte, "**MPA: Model-assisted PCB Attestation via Board-level RO and Temperature Compensation**," IEEE Asian Hardware-Oriented Security and Trust Symposium (AsianHOST), 2017.
172. K. Yang, H. Shen, D. Forte, and M. Tehranipoor, "**A Split Manufacturing Approach for Unclonable Chipless RFIDs for Pharmaceutical Supply Chain Security**," IEEE Asian Hardware-Oriented Security and Trust Symposium (AsianHOST), 2017.
173. E.L. Principe, N. Asadizanjani, D. Forte, M. Tehranipoor, R. Chivas, M. DiBattista, S. Silverman, M. Marsh, J. Mastovich, J. Odum, "**Steps Towards Automated Deprocessing of Integrated Circuits**," International Symposium on Test and Failure Analysis (ISTFA), 2017. **Received Outstanding Paper Award.**
174. A. Nahiyani, M. Sadi, R. Vittal, G. Contreras, D. Forte, and M. Tehranipoor, "**Hardware Trojan Detection Through Information Flow Security Verification**," International Test Conference (ITC), 2017.
175. X. Xu, B. Shakiya, M. Tehranipoor, and D. Forte, "**Novel Bypass Attack and BDD-based Tradeoff Analysis Against all Known Logic Locking Attacks**," Conference on Cryptographic Hardware and Embedded Systems (CHES), 2017.
176. Z. Guo, M. Tehranipoor, and D. Forte, "**Memory-based Counterfeit IC Detection Framework**," SRC TECHCON, 2017.
177. A. Nahiyani, D. Forte, and M. Tehranipoor, "**Framework for Automated and Systematic Security Assessment of Modern SoCs**," SRC TECHCON, 2017.
178. J. Park, M. Corba, A. E. de la Serna, R. Vigeant, M. Tehranipoor, and S. Bhunia, "**ATAVE: A Framework for Automatic Timing Attack Vulnerability Evaluation**," IEEE Mid-West Symposium on Circuits and Systems (MWSCAS), 2017.
179. S. Amir, B. Shakiya, D. Forte, M. Tehranipoor, and S. Bhunia, "**Comparative Analysis of Hardware Obfuscation for IP Protection**," ACM Great Lake Symposium on VLSI (GLS-VLSI), 2017.
180. Q. Shi, K. Xiao, D. Forte, and M. Tehranipoor, "**Securing Split Manufactured ICs with Wire Lifting Obfuscated Built-In Self-Authentication**," ACM Great Lake Symposium on VLSI (GLS-VLSI), 2017.
181. M. Sadi, S. Kannan, and M. Tehranipoor, "**Design of a Digital IP for 3D-IC Die-to-Die Clock Synchronization**," IEEE International Symposium on Circuits & Systems (ISCAS), 2017.
182. Z. Guo, M. Tehranipoor, and D. Forte, "**FFD: A Framework for Fake Flash Detection**," Design Automation Conference (DAC), 2017.
183. T. Bryant, S. Chowdhury, D. Forte, M. Tehranipoor and N. Maghari, "**A Stochastic All-Digital Weak Physically Unclonable Function for Analog/Mixed-Signal Applications**," IEEE Int. Symposium on Hardware-Oriented Security and Trust (HOST), 2017.
184. N. Karimian, M. Tehranipoor, and D. Forte, "**Non-Fiducial PPG-based Authentication for Healthcare Application**," Engineering in Medicine and Biology Conference (EMBC), 2017.
185. N. Karimian, M. Tehranipoor, and D. Forte, "**Noise Assessment Framework for Optimizing ECG Key Generation**," International Conference on Technologies for Homeland Security, 2017.

186. D. Zhang, X. Wang, T. He, and M. Tehranipoor, "**A Novel Dynamic Obfuscation Scan Design for Protecting IPs against Scan-Based Attack**," IEEE VLSI Test Symposium (VTS), 2017.
187. Q. Shi, N. Asadi, D. Forte, and M. Tehranipoor, "**Layout-based Microprobing Vulnerability Assessment for Security Critical Applications**," GOMACTech, 2017.
188. N. Karimian, Z. Guo, M. Tehranipoor, and D. Forte, "**Human Recognition from Photoplethysmography (PPG) Based on Non-fiducial Features**," IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP), 2017.
189. G. K. Contreras, A. Nahiyan, S. Bhunia, D. Forte, M. Tehranipoor, "**Security Vulnerability Analysis of Design-for-Test Exploits for Asset Protection in SoCs**," Asia and South Pacific Design Automation Conference (ASP-DAC), 2017.
190. R. Karam, T. Hoque, S. Ray, M. Tehranipoor, S. Bhunia, "**MUTARCH: Architectural Diversity for FPGA Device and IP Security**," Asia and South Pacific Design Automation Conference (ASP-DAC), 2017.
191. Z. Guo, M. Tehranipoor, and D. Forte, "**Aging Attacks for Key Extraction on Permutation-Based Obfuscation**," IEEE Asian Hardware-Oriented Security and Trust (AsianHOST), 2016.
192. T. Rahman, D. Forte, X. Wang, and M. Tehranipoor, "**Enhancing Noise Sensitivity of Embedded SRAMs for Robust True Random Number Generation in SoCs**," IEEE Asian Hardware-Oriented Security and Trust (AsianHOST), 2016.
193. R. Karam, T. Hoque, S. Ray, M. Tehranipoor and S. Bhunia, "**Robust Bitstream Protection in FPGA-based Systems through Low-Overhead Obfuscation**," ReConFig 2016.
194. M. Sadi, G. Contreras, D. Tran, J. Chen, L. Winemberg, and M. Tehranipoor, "**BIST-RM: BIST-Assisted Reliability Management of SoCs Using On-Chip Clock Sweeping and Machine Learning**," International Test Conference (ITC), 2016.
195. M. Alam, M. Tehranipoor, and D. Forte, "**Recycled FPGA Detection using Exclusive LUT Path Delay Characterization**," International Test Conference (ITC), 2016.
196. T. Bryant, S. Chowdhury, D. Forte, M. Tehranipoor, and N. Maghari, "**A Stochastic Approach to Analog Physical Unclonable Function**," IEEE Midwest Symposium on Circuits and Systems (MWSCAS), 2016.
197. B. Shakya, N. Asadi, D. Forte, and M. Tehranipoor, "**Chip Editor: leveraging Circuit Edit for Logic Obfuscation and Trusted Fabrication**," IEEE International Conference on Computer-Aided Design (ICCAD), 2016.
198. N. Karimian, D. Woodard, M. Tehranipoor, and D. Forte, "**Biometrics for Authentication in Resource-Constrained Systems**," Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC), 2016.
199. G. Contreras and M. Tehranipoor, "**Fault Deterministic Vector Analysis and Seed Extraction for LBIST**," SRC TECHCON, 2016. **Received Best in Session Award.**
200. M. He and M. Tehranipoor, "**Test-Point Insertion Efficiency Analysis for LBIST Applications**," SRC TECHCON, 2016.
201. M. Sadi and M. Tehranipoor, "**BIST-Assisted In-field Aging Reliability Management of SoCs Using On-Chip Clock Sweeping and Machine Learning**," SRC TECHCON, 2016. **Received Best in Session Award.**
202. T. Rahman, D. Forte, and M. Tehranipoor, "**SRAM Inspired Design and Optimization for Developing Robust Security Primitives**," SRC TECHCON, 2016. **Received Best in Session Award.**
203. N. Asadizanjani, D. Forte, and M. Tehranipoor, "**Non-destructive Bond Pull and Ball Shear Failure Analysis Based on Real Structural Properties**," Int. Symposium on Testing and Failure Analysis (ISTFA), 2016.
204. N. Asadizanjani, H. Chen, B. Shakya, D. Forte, S. Bhunia, and M. Tehranipoor, "**A New Methodology to Protect PCBs from Non-destructive Reverse Engineering**," Int. Symposium on Testing and Failure Analysis (ISTFA), 2016.

205. N. Asadizanjani, S. Gattigowda, N. Dunn, D. Forte, and M. Tehranipoor, "**A Database for Counterfeit Electronics and Automatic Defect Detection Based on Image processing and Machine Learning**," Int. Symposium on Testing and Failure Analysis (ISTFA), 2016.
206. S. Ray, S. Bhunia, Y. Jin, and M. Tehranipoor, "[Extended Abstract] **Security Validation in IoT Space**," IEEE VLSI Test Symposium (VTS), 2016.
207. H. Shen, F. Rahman, B. Shakya, M. Tehranipoor, and D. Forte, "**Selective Enhancement of Randomness at the Materials Level: Poly-Si Based Physical Unclonable Functions (PUFs)**," IEEE Computer Society Annual Symposium on VLSI (ISVLSI) 2016.
208. T. Li, J. Di, M. Tehranipoor, D. Forte, and L. Wang, "**Tracking Data Flow at Gate-Level through Structural Checking**," ACM GLS-VLSI, 2016.
209. A. Zaghi and Mark Tehranipoor, "**Major Observations from a Specialized REU Program for Engineering Students with ADHD**," American Society for Engineering Education (ASEE), 2016.
210. F. Rahman, D. Forte, and Mark Tehranipoor, "**Reliability vs. Security: Challenges and Opportunities for Developing Reliable and Secure Integrated Circuits**," International Reliability Physics Symposium (IRPS), 2016.
211. M. Sadi and M. Tehranipoor, "**BIST-Assisted Reliability Management of SoC Using On-chip Clock Sweeping and Machine Learning**," IEEE Reliability Innovations Conference (IRIC), 2016 (extended abstract).
212. K. Yang, D. Forte, and M. Tehranipoor, "**UCR: An Unclonable Chipless RFID Tag**," IEEE Symposium on Hardware-Oriented Security and Trust (HOST), 2016.
213. Q. Shi, N. Asadi, D. Forte, and M. Tehranipoor, "**A Layout-driven Framework to Assess Vulnerability of ICs to Microprobing Attacks**," IEEE Symposium on Hardware-Oriented Security and Trust (HOST), 2016. (Best Paper Award)
214. Z. Guo, T. Rahman, M. Tehranipoor, and D. Forte, "**A Zero-cost Approach to Detect Recycled SoC Chips Using Embedded SRAM**," IEEE Symposium on Hardware-Oriented Security and Trust (HOST), 2016. (Best Paper Nominate)
215. A. Nahiyani, K. Xiao, K. Yang, D. Forte, Y. Jin, and M. Tehranipoor, "**AVFSM: A Framework for Identifying and Mitigating Vulnerabilities in FSMs**," Design Automation Conference (DAC), 2016.
216. Z. Guo, N. Karimian, M. Tehranipoor, and D. Forte, "**Hardware Security Meets Biometrics for the Age of IoT**," Int. Symposium on Circuits and Systems (ISCAS), 2016.
217. T. Meade, Y. Jin, M. Tehranipoor, S. Zhang, "**Gate-Level Netlist Reverse Engineering for Hardware Security: Control Logic Register Identification**," Int. Symposium on Circuits and Systems (ISCAS), 2016.
218. L. Yu, X. Wang, P. Jiao, A. Chen, D. Su, L. Winemberg, M. Sadi, and M. Tehranipoor, "**An Efficient All-Digital Alarmer for DVFS-based SOC**," Int. Symposium on Circuits and Systems (ISCAS), 2016.
219. L. Wu, X. Wang, D. Su, A. Chen, Q. Shi, and M. Tehranipoor, "**AES Design Improvement Toward Information Safety**," Int. Symposium on Circuits and Systems (ISCAS), 2016.
220. M. He, G. Contreras, M. Tehranipoor, D. Tran, and L. Winemberg, "**Test Point Insertion Efficiency Analysis for LBIST Applications**," IEEE VLSI Test Symposium (VTS), 2016.
221. T. Meade, S. Zhang, M. Tehranipoor, and Y. Jin, "**A Comprehensive Netlist Reverse Engineering Toolset for IC Trust**," GomacTech, 2016.
222. N. Asadi, S. Shahbazi, D. Forte, and M. Tehranipoor, "**Nondestructive X-ray Tomography Based Bond Pull and Ball Shear Analysis**," GomacTech, 2016.
223. Z. Guo, N. Karimian, M. Tehranipoor, and D. Forte, "**Biometric Based Human-to-Device (H2D) Authentication**," GomacTech, 2016.
224. M. Alam, N. Asadi, S. Shahbazi, D. Forte, and M. Tehranipoor, "**The Impact of X-ray Tomography on the Reliability of FPGAs**," GomacTech, 2016.
225. B. Shakya, F. Rahman, M. Tehranipoor, and D. Forte, "**Security in Nanoscale Regime – A Perspective Paper**," IEEE Microprocessor Test and Verification (MTV), 2015.

226. K. Ahi, N. Asadi, M. Tehranipoor, and M. Anwar, “**Authentication of electronic components by time domain THz Techniques**,” Connecticut Microelectronic Symposium (CMOC), 2015 (extended abstract).
227. K. Yang, D. Forte, and M. Tehranipoor, “**Protecting Endpoint Devices in IoT Supply Chain**,” International Conference on Computer-Aided Design (ICCAD), 2015.
228. Q. Shi, R. Tekumalla, and M. Tehranipoor, “**Concurrent Testing of Logic and Memory, and Detection of Memory Functional Paths in SOCs**,” International Test Conference, 2015 (invited).
229. B. Shakya, U. Guin, M. Tehranipoor, and D. Forte, “**Performance Optimization for On-Chip Sensors to Detect Recycled ICs**,” IEEE Int. Conference on Computer Design (ICCD), 2015.
230. T. Rahman, F. Rahman, D. Forte, and M. Tehranipoor, “**A Pair Selection Algorithm for Robust RO-PUF Against Environmental Variations and Aging**,” IEEE Int. Conference on Computer Design (ICCD), 2015.
231. G. Contreras, L. Winemberg, M. Tehranipoor, and N. Ahmed, “**Predictive LBIST Model and partial ATPG for Seed Extraction**,” IEEE Defect and Fault Tolerant Systems (DFTS), 2015.
232. S. Chen, J. Chen, D. Forte, J. Di, M. Tehranipoor, and L. Wang, “**Chip Level Anti-reverse Engineering using Transformable Interconnects**,” IEEE Defect and Fault Tolerant Systems (DFTS), 2015.
233. N. Asadi, S. Shahbaz, M. Tehranipoor, and D. Forte, “**Non-destructive PCB Reverse Engineering Using X-ray Micro Computed Tomography**,” Int. Symposium for Testing and Failure Analysis (ISTFA), 2015.
234. H. Dogan, N. Asadi, S. Shahbaz, D. Forte, and M. Tehranipoor, “**Analyzing the Impact of X-ray Tomography for Non-destructive Counterfeit Detection**,” Int. Symposium for Testing and Failure Analysis (ISTFA), 2015.
235. K. Ahi, N. Asadi, S. Shahbaz, M. Tehranipoor, and M. Anwar, “**Terahertz Characterization of Electronic Components and Comparison of Terahertz Imaging with X-ray Imaging Techniques**,” Terahertz Physics, Devices, and Systems, 2015.
236. K. Yang, D. Forte, and M. Tehranipoor, “**ReSC: RFID-enabled Supply Chain Management and Traceability for Network Devices**,” RFID Security, 2015.
237. T. Rahman, D. Forte, and M. Tehranipoor, “**Robust SRAM-PUF: Cell Stability Analysis and Novel Bit-Selection Algorithm**,” TECHCON, 2015.
238. M. Sadi and M. Tehranipoor, “**An Efficient Speed Binning Methodology for SoC Using On-chip Slack Sensors and Machine Learning**,” TECHCON, 2015.
239. J. Chandy, et. al, “**Hardware Hacking: An Approach to Trustable Computing Systems Security Education**,” The Colloquium for Information Systems Security Education (CISSE). Las Vegas, June 2015.
240. Z. Guo, J. Di, M. Tehranipoor, and D. Forte, “**Investigation of Obfuscation-based Anti-Reverse Engineering for Printed Circuit Boards**,” Design Automation Conference (DAC), 2015.
241. M. Sadi, X. Wang, L. Winemberg, and M. Tehranipoor, “**Speed Binning using Machine Learning and On-chip Slack Sensors**,” ACM Great Lake Symposium on VLSI (GLSVLSI), 2015.
242. M. Sadi and M. Tehranipoor, “**Timing Slack Extraction for SoC Reliability Monitoring with Robust Digital Sensor IP and Sensor Insertion Flow**,” IEEE Reliability Innovations Conference (IRIC), 2015 (extended abstract).
243. T. Rahman, A. Hosey, K. Xiao, D. Forte, and M. Tehranipoor, “**Cell Stability Analysis and Novel Bit-Selection Algorithm for Robust SRAM-PUF**,” Connecticut Microelectronic Symposium (CMOC), 2015 (extended abstract).
244. M. Sadi and M. Tehranipoor, “**A Robust Multipurpose Digital Sensor IP for In-situ Path Timing Slack Monitoring in SOCs**,” IEEE VLSI Test Symposium (VTS), 2015.
245. K. Xiao, D. Forte, and M. Tehranipoor, “**Efficient and Secure Split Manufacturing via Obfuscated Built-In Self-Authentication**,” IEEE Hardware-Oriented Security and Trust (HOST), 2015. (Best Paper Award)

246. K. Yang, D. Forte, and M. Tehranipoor, "**An RFID-based Technology for Electronic Component and System Counterfeit Detection and Traceability**," IEEE International Conference on Technologies for Homeland Security (HST), 2015.
247. G. Contreras, M. Tehranipoor, N. Ahmed, L. Winemberg, and Y. Zhao, "**LBIST Pattern Reduction by Learning ATPG Test Cube Properties**," International Symposium on Quality Electronic Design (ISQED), 2015.
248. S. Quadir, N. Asadi, D. Forte, and M. Tehranipoor, "**Rapid Non-destructive Reverse Engineering of Printed Circuit Boards by High Resolution X-ray Tomography**," GOMACTech, 2015.
249. T. Rahman, A. Hosey, F. Rahman, D. Forte, and M. Tehranipoor, "**RePa: A Pair Selection Algorithm for Reliable Keys from RO-based PUF**," GOMACTech, 2015.
250. H. Dogan, D. Forte, and M. Tehranipoor, "**Aging Analysis for Recycled FPGA Detection**," GOMACTech, 2015.
251. M. Sadi, Z. Conroy, B. Eklow, M. Kamm, N. Bidokhti, and M. Tehranipoor, "**An All-Digital Distributed Sensor Network Based Framework for Continuous Noise Monitoring and Timing Failure Analysis in SOCs**" IEEE Asian Test Symposium (ATS), pp. 269-274, 2014.
252. A. Hosey, T. Rahman, K. Xiao, D. Forte, and M. Tehranipoor, "**Advanced Analysis of Cell Stability for Reliable SRAM PUFs**," IEEE Asian Test Symposium (ATS), pp. 348-358, 2014.
253. H. Dogan, D. Forte, and M. Tehranipoor, "**Aging Analysis for Recycled FPGA Detection**," IEEE Int. Symposium on Defect and Fault Tolerance Symposium (DFTS), pp. 171-76, 2014.
254. M. He and M. Tehranipoor, "**SAM: A Comprehensive Mechanism for Accessing Embedded Sensors in Modern SoCs**," IEEE Int. Symposium on Defect and Fault Tolerance Symposium (DFTS), pp. 240-246, 2014.
255. T. Rahman, D. Forte, Q. Shi, G. Contreras, and M. Tehranipoor, "**CSST: Preventing Distribution of Unlicensed and Rejected ICs by Untrusted Foundry and Assembly**," IEEE Int. Symposium on Defect and Fault Tolerance Symposium (DFTS), pp. 46-51, 2014.
256. M. Sadi and M. Tehranipoor, "**A SOC Noise Monitoring and Diagnosis with Fully Digital On-Chip Distributed Sensor Network**," SRC TECHCON 2014.
257. G. Contreras and M. Tehranipoor, "**Improving LBIST Pattern Quality and Test Point Reduction**," SRC TECHCON 2014.
258. Q. Shi, X. Wang, L. Winemberg, and M. Tehranipoor, "**On-Chip Sensor Selection for Effective Speed-Binning**," IEEE Mid-West Symposium on Circuits and Systems (MWSCAS), Oct. 2014.
259. S. Shahbaz, D. Forte, and M. Tehranipoor, "**Advanced Physical Inspection Methods for Counterfeit Detection**," Int. Symposium for Testing and Failure Analysis (ISTFA), pp. 1073-1076, 2014 (**Best Paper Candidate**).
260. S. Shahbaz, D. Forte, and M. Tehranipoor, "**Advanced Physical Inspection Techniques for Counterfeit IC Detection**," Calce Symposium on Counterfeit Electronics and Supply Chain, pp. 55-64, 2014.
261. G. Contreras, N. Ahmed, L. Winemberg, and M. Tehranipoor, "**TAME-TPI: A Timing-Aware Metric for Efficient Test Point Insertion and Area Overhead Reduction**," IEEE North Atlantic Test Workshop (NATW), 2014.
262. T. Rahman, D. Forte, Q. Shi, G. Contreras, and M. Tehranipoor, "**CSST: An Efficient Secure Split-Test for Preventing IC Piracy**," IEEE North Atlantic Test Workshop (NATW), pp. 43-47, 2014.
263. X. Wang, L. Winemberg, A. Haggag, J. Chayachinda, A. Saluja and M. Tehranipoor, "**Fast Aging Degradation Rate Prediction During Production Test**," International Reliability Physics Symposium (IRPS), pp. 6B.5.1-6B.5.5, 2014.
264. M. Sadi and M. Tehranipoor, "**On-Chip Sensors for Chip Timing Failure Analysis**", Connecticut Symposium on Microelectronics and Optoelectronics (CMOC), 2014.
265. M. Sadi, Z. Conroy, M. Kamm, B. Eklow, N. Bidokhti and M. Tehranipoor "**System on Chip Noise Reliability Testing and Monitoring with Light-Weight Fully Digital Embedded Sensor Network**" IEEE International Reliability Innovation Conference (IRIC), 2014.

266. K. Xiao, T. Rahman, D. Forte, M. Tehranipoor, M. Su, and Y. Huang, "**Bit Selection Algorithm Suitable for High Volume Production of SRAM PUF**," IEEE International Symposium on Hardware-Oriented Security and Trust (HOST), pp. 101-106, 2014.
267. T. Rahman, K. Xiao, D. Forte, X. Zhang, Z. Shi, and M. Tehranipoor, "**TI-TRNG: Technology Independent True Random Number Generator**," Design Automation Conference (DAC), 2014.
268. U. Guin, X. Zhang, D. Forte, and M. Tehranipoor, "**Low-Cost On-Chip Structures for Combating Die and IC Recycling**," Design Automation Conference (DAC), 2014.
269. J. Chen, L. Winemberg, and M. Tehranipoor, "**Identification of Testable Representative Paths for Low-Cost Verification of Circuit Performance During Manufacturing Tests and in the Field**," IEEE VLSI Test Symposium (VTS), 2014.
270. S. Hamdiui, G. Di Natalie, G. van Battum, J. Danger, F. Smailbegovic, and M. Tehranipoor, "**Hacking and Protecting IC Hardware**," Design, Automation, and Test in Europe (DATE), 2014.
271. T. Rahman, D. Forte, M. Tehranipoor, and J. Fahrny, "**ARO-PUF: An Aging-Resistant Ring-Oscillator PUF Design**," Design, Automation, and Test in Europe (DATE), pp. 1-6, 2014.
272. K. Xiao, T. Rahman, D. Forte, M. Tehranipoor, Y. Huang, and M. Su, "**Low-cost Analysis of SRAM PUFs for Identification of Mass-Produced Electronic Devices**," GOMACTech, 2014.
273. U. Guin, D. Forte, D. DiMase, and M. Tehranipoor, "**Counterfeit IC Detection: Test Method Selection Considering Test Time, Cost, and Tier Level Risk**," GOMACTech, 2014.
274. U. Guin, D. Forte, and M. Tehranipoor, "**Low-cost On-Chip Structures for Combating Die and IC Recycling**," GOMACTech, 2014.
275. N. Bidokhti, M. Tehranipoor, J. Chen, and J. Lee, "**Life After Failure**," Reliability and Maintainability Symposium (RAMS), 2014.
276. U. Guin, D. Forte, and M. Tehranipoor, "**Anti-Counterfeit Techniques: From Design to Resign**," IEEE Microprocessor Test Verification (MTV), pp. 89-94, 2013.
277. J. Chen and M. Tehranipoor, "**Critical Paths Selection and Test Cost Reduction Considering Process Variations**," IEEE Asian Test Symposium (ATS), pp. 259 - 264, 2013.
278. F. Bao, H. Chen, and M. Tehranipoor, "**Worst-case Critical-Path Delay Analysis Considering Power-Supply Noise**," IEEE Asian Test Symposium (ATS), pp. 37-42, 2013.
279. A. Tomita, X. Wen, Y. Sato, S. Kajihara, P. Girard, M. Tehranipoor, and L.T. Wang, "**On Achieving Capture Power Safety in At-speed Scan-based Logic BIST**," IEEE Asian Test Symposium (ATS), pp. 19-24, 2013.
280. U. Guin and M. Tehranipoor, "**CDIR: Low-Cost Combating Die/IC Recycling Structures**," DMSMS, 2013 (Invited)
281. U. Guin, D. DiMase, and M. Tehranipoor, "**CDC: Counterfeit Defect Coverage Analysis**," DMSMS, 2013 (Invited)
282. A. Mazady, H. Chi Chou, M. Tehranipoor and M. Anwar, "**Terahertz Spectroscopy: A Technology Platform for the Detection of Counterfeit Electronics**," DMSMS, 2013 (Invited)
283. U. Guin, T. Chakraborty, and M. Tehranipoor, "**Novel DFTs for Circuit Initialization to Reduce Functional Fmax Test Time**," IEEE Int. Conference on Computer Design (ICCD), 2013.
284. H. Salmani, M. Tehranipoor, and R. Karri, "**Trust Benchmark and Design Vulnerability Analysis**," IEEE Int. Conference on Computer Design (ICCD), 2013.
285. G. Contreras, T. Rahman, and M. Tehranipoor, "**Secure Split-Test for Preventing IC Piracy by Untrusted Foundry and Assembly**," Int. Symposium on Defect and Fault Tolerance in VLSI Systems (DFT), pp. 196-203, 2013.
286. H. Salmani and M. Tehranipoor, "**Analyzing Circuit Vulnerability to Hardware Trojan Insertion at the Behavioral Level**," Int. Symposium on Defect and Fault Tolerance in VLSI Systems (DFT), pp. 190-195, 2013.
287. Q. Shi, J. Chen, and M. Tehranipoor, "**Silicon Data Based Delay Analysis and PDF Pattern Generation for Advanced Technology Node**," SRC TECHCON, September 2013.
288. M. Tehranipoor, "**An All-in-One Anti-Counterfeiting Technology for Integrated Circuits**," Symposium on Counterfeit Electronic Parts and Electronic Supply Chain, 2013.

289. Q. Shi, X. Wang, L. Winemberg, and M. Tehranipoor, "**Experimental Analysis of Variations' Impact on Integrated Circuits Performance in Advanced Technology Nodes,**" North Atlantic Test Workshop (NATW), 2013.
290. U. Guin, T. Chakraborty, and M. Tehranipoor, "**Novel DFTs for Circuit Initialization to Reduce Functional Fmax Test Time,**" North Atlantic Test Workshop (NATW), 2013.
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423. M. H. Tehranipour, N. Ahmed and M. Nourani, "**Multiple Transition Model and Enhanced Boundary Scan Architecture to Test Interconnects for Signal Integrity**," in proc. IEEE International Conference on Computer Design (ICCD'03), San-Jose, CA, pp. 554-559, 2003.
424. M. H. Tehranipour, M. Nourani and S. M. Fakhraie, "**Systematic Test Program Generation for SoC Testing Using Embedded Processor**," in proc. IEEE International Symposium on Circuits And Systems (ISCAS'03), Bangkok, Thailand, vol. 5, pp. 541-544, 2003.
425. G. R. Chaji, R. M. Pourrad, S. M. Fakhraie and M. H. Tehranipour, "**eUTDSP: A Design Study of a New VLIW-Based DSP Architecture**," in proc. IEEE International Symposium on Circuits And Systems (ISCAS'03), Bangkok, Thailand, vol. 4, pp. 137-140, 2003.
426. M. H. Tehranipour and M. Nourani, "**Signal Integrity Loss in SoC's Interconnects: A Diagnostic Approach Using Embedded Microprocessor**," in proc. IEEE International Test Conference (ITC'02), Baltimore, MD, pp. 1093-1102, 2002.
427. S. M. Fakhraie, M. H. Tehranipour, M. R. Movahedin and M. Nourani, "**Fast Prototyping of a DSP Core**," in proc. IEEE MidWest Symposium on Circuits and Systems (MWSCAS'02), Tulsa, Oklahoma, vol. 2, pp. 215-218, 2002.
428. M. H. Tehranipour, M. Nourani, S. M. Fakhraie and C. A. Papachristou, "**Test Optimization of Bus-Structured SoCs Using Embedded Microprocessor**," in proc. IEEE MidWest Symposium on Circuits and Systems (MWSCAS'02), Tulsa, Oklahoma, vol. 1, pp. 168-171, 2002.

429. M. Tehranipour, Z. Navabi and S. M. Fakhraie, “**An Efficient BIST for Embedded SRAM Testing**,” in proc. IEEE International Symposium on Circuits and Systems (ISCAS'01), Sydney, Australia, Vol 5, pp. 73-76, 2001.
430. M. Tehranipour, Z. Navabi and S. M. Fakhraie, “**A Low-Cost BIST Architecture for Processor Cores**,” in proc. IEEE Electronic Circuits and Systems Conference (ECS'01), Bratislava, Slovakia, pp. 11-14, 2001.
431. M. Tehranipour and Z. Navabi, “**Zero-Overhead BIST for Internal SRAM Testing**,” in proc. IEEE International Conference on Microelectronics (ICM'00), Tehran, Iran, pp. 109-112, 2000.

Technical Reports and Invited Poster Presentations

1. U. Guin, M. Tehranipour, D. DiMase, and M. Megrđician, “**Counterfeit IC Detection and Challenges Ahead**,” ACM SIGDA, March 2013.
2. N. Reddy and M. Tehranipour, “**Reliability Analysis for 90nm Test Chips**,” Technical Reports, CADT-20110110, 2011.
3. F. Wu, L. Dilillo, A. Bosio, P. Girard, S. Pravossoudovitch, A. Virazel, M. Tehranipour, K. Miyase, X. Wen, N. Ahmed, “**Is Test Power Reduction Through X-Filling Good Enough?**,” Poster presentation, Int. Test Conference (ITC), 2010.
4. J. Lee and M. Tehranipour, “**Low-power Transition Delay Fault Test Pattern Generation**,” IEEE VLSI Test Symposium (VTS), 2008, PhD Thesis Poster Presentation.
5. M. Tehranipour, “**Trojan Detection and Isolation in Integrated Circuits**,” NSF Cyber Trust meeting, New Haven, March 2008
6. N. Ahmed, M. Tehranipour, and V. Jayaram, “**Considering IR-Drop Effects During Faster-than-at-Speed Delay Test**,” presented in Special Session (Elevator Talk), IEEE VLSI Test Symposium (VTS), 2006.
7. N. Ahmed and M. Tehranipour, “**On-chip Scan Enable Generation for Transition Fault Testing**,” Poster Presentation, University Booth, ITC 2005.
8. J. Plusquellic, D. Acharyya, C. Patel, A. Singh and M. Tehranipour, “**Hardware Investigation of Defect Sensitivity of a Multiple Supply Pad IDDQ Method**,” Poster Presentation, University Booth, ITC 2005.
9. N. Ahmed and M. Tehranipour, “**Enhanced Launch-off-Capture with Improved Fault Coverage and Reduced Pattern Count**,” Presented in UT-Austin Poster Session, ITC 2005.
10. M. H. Tehranipour and M. Nourani, “**Low-Power Test pattern generation for BIST Architecture**,” University of Texas at Dallas, 2003.
11. M. H. Tehranipour and M. Nourani, “**Test Compression and Power Reduction in Scan Using RL-Huffman Encoding**,” University of Texas at Dallas, 2002.

Consulting

1. **Consulting** with many companies (OCMs, OEMs, and EDA) and universities worldwide
2. Served on the **advisory board** of several companies with focus on cybersecurity

Invited Talks and Keynote Addresses (~240)

- **Distinguished Professor Lecture Series**, March 12, 2026
- **SEMI**, Jan 22, 2026, Pager Attacks: How it happened?
- **Keynote Address**, LightSec Workshop, Istanbul, Turkey, 2025
- **SkyTalk**, Design Automation Conference (DAC), 2025
- **Invited Talk**, US-Japan Hardware Security Workshop
- **Keynote Address**, Secure Heterogeneous Integration and Advanced packaging: New Attack Surfaces and Grand Challenges, IEEE VLSI Design, 2024.
- **Keynote Address**, KIAT-UF-BRIDG Semiconductor Workshop, Seoul, Korea

- **Invited Talk**, NIST Assurance Workshop, March 2024
- **Invited Talk**, Seoul National University, Jan 2024
- **Keynote Address**, VLSID, Kolkata, India, Jan. 2024
- **Keynote Address**, Hardware Security Forum, National Taiwan University, Taiwan, Dec. 2023
- **Invited Talk**, National Chiao Tung University, Taiwan, Dec. 2023
- **Invited Talk**, MediaTek, Taiwan, Dec. 2023
- **Keynote Address**, IEEE DFTS, October 2023, Nice, France
- **Invited Talk**, University of Minnesota, September 2023
- **Keynote Address**, GLS-VLSI, May 2023, Knoxville, Tennessee
- **Keynote Address**, IEEE International Symposium on Hardware-Oriented Security and Trust (**HOST**), San Jose, May 2023
- **Jack Kilby Keynote Address**, GomacTech, San Diego, March 2023
- **Keynote Address**, RISE Workshop, London, Dec. 2023
- **Invited Talk**, SRC HWS e-Workshop, Hardware Security: A Vision for the Next Decade, May 2022
- **Invited Talk**, Accellera IPSA, Quantifiable Assurance: From IPs to SoCs, April 19, 2022
- **Visionary Talk**, Silicon Lifecycle Management (SLM) Workshop, March 18, 2022
- **Invited Talk**, Intel, Quantifiable Assurance: From IPs to SoCs, Feb. 2022
- **Keynote Address**, Synopsys User Group, SNUG, March, 2022
- **Invited Talk**, NIST, State of the Microelectronics Security and Trust, Jan 2022
- Interview with Dr. Jay Lewis, Partner, Microsoft, 2021
- Interview with Serge Leef, MTO Program Manager, DARPA, MEST Center, 2021
- Interview with Dr. Wally Rhines, CEO of CORNAMI, MEST Center, 2021
- **Invited Speaker**, Microelectronics Packaging & Test Engineering Council (MEPTEC), Nov. 3, 2021 (https://www.youtube.com/watch?v=SQLgdezOw_Q&t=4s)
- **Keynote Address**, Workshop on RTL and High Level Testing (WRTLTL), Nov. 2021
- **Invited Talk**, UF AI Speaker Series, Nov. 2021 (<https://www.youtube.com/watch?v=gZxyb45jnLM>)
- **Invited Talk**, Dynetics, Nov. 2021
- **Invited Talk**, Design Automation Conference (DAC), Dec. 2021
- **Keynote Address**, IEEE Microelectronics Design and Test Symposium (MDTS), May 2021
- **Keynote Address**, Workshop on Securing the Nation's 5G Supply Chain Through Measurement Countermeasure, NIST, 2021
- **Invited Talk**, Microsoft, Title: State of the Microelectronics Security, March 2021
- **Keynote Address**, ACM Workshop on Attacks and Solutions for Hardware Security (**ASHES**), November 2020
- **Invited Talk**, KBR Center of Excellence on Microelectronic Trust, October 16, 2020
- **Invited Talk**, NIST's Cybersecurity and Privacy Federal Advisory Board, October 15, 2020
- **Keynote Address**, MOST (Ministry of Science and Technology, R.O.C.), ESD Alliance and SEMI, Security on Chip Summit in **SEMICON** Taiwan on September 25th, 2020 in TaiNEX1, Taiwan.
- **Keynote Address**, International Test Conference (**ITC**) Asia, September 2020.
- **Invited Talk**, DOD Technical Executives, Education and Workforce Development, Aug, 2020
- **Invited Talk**, Cyber Security and Information Assurance (CSIA) IWG, Aug. 2020
- **Keynote Address**, SRC/SIA/DoE Decadal Plan workshop on ICT Hardware Enabled Security, Aug, 26, 2020
- **Invited Talk**, ACM SIGDA / IEEE CEDA webinar, Design Automation WebiNar (**DAWN**), Title: *Automatic Implementation of Secure Silicon (AISS)*, Aug 2020
- **Invited Talk**, Global Foundries Executive Talk, July 2020
- **Invited Talk**, Texas Instruments Gator Day, July 2020

- **Invited Talk**, IEEE Oregon Section, The Pursuit of Happyness: Root of Trust for Cybersecurity, June 2020
- **Invited Talk**, DARPA, Automated Rule Checking for Hardware Security, May 2020
- **Keynote Address**, Cyber Resilient Supply Chain Technologies (**CReSCT**), May 2020
- **Invited Webinar**, MEST Center, Title: Supply Chain Security, 2019
- **Invited Talk**, OSD Quantifiable Assurance (QA), Title: Quantifiable Assurance under Zero Trust, Washington DC, Oct. 2019
- **Invited Talk**, ERI Summit – Hardware Security Workshop, July 2019, Title: Securing Supply Chain from Chips to PCBs
- **Invited Talk**, Qualcomm, June 2019, SoC Supply Chain Security
- **Invited Talk**: Gator 100 Conference, March 2019
- **Keynote Address**, GomacTech 2019, Title: *The Pursuit of Happiness: Establishing hardware root of Trust for cybersecurity*
- **Invited Talk**: DARPA OMG Meeting, Feb. 2019, Title: Defense-in-Depth for Secure Obfuscation
- **Invited Talk**, NXP, Chandler, AZ, October 2018, Title: *New Trends and Challenges in Securing Hardware*
- **Keynote Address**, ISTFA 2018, Phoenix, AZ, October 2018, Title: *Hardware Root-of-Trust for Cyber Security: Uncovering the Role of Test and Failure Analysis in Enabling Cyber Defense*
- **Keynote Address**, Asian Test Symposium (ATS), Hefei, China, October 2018, Title: *Securing SoCs: Current Practices and Challenges*
- **Invited Talk**, GeorgiaTech, September 2018
- **Keynote Address**, IEEE World Conference on Information Security Applications, Jeju, Korea, August 2018
- **Invited Presentation**, GeorgiaTech, IoT Summer School, August 2018
- **Invited Talk, Distinguished Speaker Series**, Navy Crane, IN, August 2018
- **Keynote Address**, SRC Workshop on Fabrics of the Security, Fremont, CA, July 2018
- **Invited Talk**, NSF SCCS Workshop, Title: *SoC Security Validation*, Washington DC, March 2017
- **Invited Talk**, Cisco CRC workshop on Hardware Security, San Jose, CA, Dec. 2017
- **Keynote Speaker**, Groundswell Conference on Cybersecurity, Melbourne, FL, Nov. 2017
- **Invited Talk**, Qualcomm, San Diego, October 2017, Title: SoC Security
- **Invited Talk**, Tsinghua University, Beijing, October 2017, Title: *When it Comes to Security, Do not Forget about Hardware*
- **Keynote Speaker**, Int. IEEE Verification and Security Workshop (IVSW), July 2017
- **Invited Talk: Air Force Research Laboratory (AFRL)**, Dayton, OH, Title: *Trusted and Assured Microelectronics*, 2017
- **Invited Talk: Air Force Research Laboratory (AFRL)**, Dayton, OH, Title: *Test and Design-for-Anti-Counterfeit*, 2017
- **Invited Talk: Ohio State University**, Columbus, OH, Title: *When It Comes to Cybersecurity, Do Not Forget About Hardware*, 2017
- **IEEE Ambassador talk at the Harris Corporation**, Melbourne, FL, March 2017, Title: *When It Comes to Cybersecurity, Do Not Forget About Hardware*
- **RSA Conference**, San Francisco, CA, February 2017, Title: *Securing Electronic Supply Chain from Design to Resign*
- **Keynote Speaker**, IEEE Asian HOST, Dec. 2016, Taiwan, Title: Security Rule Check
- **Keynote Speaker**, Microprocessor Test and Verification (MTV) Workshop, Austin, TX, Dec. 2016, Title: Security Rule Check: A Closer Look at the Automated Test for Security
- **Global Foundries, CTO Speaker Series**, Dec. 2016
- **Invited Talk: SRC e-Workshop**, July 2016
- **Invited Talk: Chinese Academy of Science (CAS)**, June 2016

- **Keynote Speaker:** International Workshop on on Hardware Security, 2016, Organized jointly by Tsinghua University and Beihang University, **Title:** Hardware Security: Past, Present, and the Future
- **Invited Talk: Peking University**, June 2016
- **Invited Talk: Beihang University**, June 2016
- **Invited Talk, Dagstuhl Seminar**, Germany, May 2016
- **Invited Talk: IEEE International Reliability Physics Symposium (IRPS)**, 2016, **Title:** *Security vs. Reliability: Where Do These Two Road Converge?*
- **Keynote Speaker: IEEE Workshop on CPS Security**, April 2016
- **Keynote Speaker: US-Brazil Joint Workshop on Cybersecurity**, April 2016, Orlando, FL
- **Invited Talk: Florida Institute of Technology (FIT)**, Host: Dr. Fareena Saqib, March 2016
- **Invited Talk: Florida Energy Systems Consortium (FESC)**, March 2016
- **Keynote Speaker: International Symposium on Quality Electronic Design (ISQED)**, Santa Clara, March 2016, **Title:** *New Frontiers in Hardware Security and Trust*
- **Invited Talk: Northrop Grumman**, Nov. 2015
- **Invited Talk: IEEE/ACM International Conference on Computer-Aided Design (ICCAD)**, Nov. 2015, Austin, TX
- **Invited Talk: Potomac Institute for Policy (PIP)**, October 2015
- **Invited Talk: DHS Software and Supply Chain Assurance Forum**, Sep. 2015
- **NSF WATCH Talk**, July 2015, Host: Jeremy Epstein
- **Invited Talk: Global Foundries**, Malta, NY, Dec. 2014
- **Keynote Speaker: Freescale Semiconductors' Technical Enrichment Conference**, Austin, TX, Dec. 2014
- **Invited Talk: Cadence**, Austin, TX, Dec. 2014
- **Invited Talk: Missile Defense Agency (MDA)**, Nov. 2014, Huntsville, Alabama
- **Invited Talk: Beihang University**, Nov. 2014, HOST: Prof. Michel Wang
- **Invited Talk: IEEE Asian Test Symposium (ATS)**, Nov. 2014
- **Invited Talk: Army Research Office (ARO) Workshop**, NYC, Nov. 2014
- **Invited Talk: CSI CyberSEED event**, University of Connecticut, Oct. 2014
- **Invited Talk: Honeywell International**, Oct. 2014
- **Invited Talk: ISE Northeast**, Oct. 2014, NYC
- **Invited Talk: Sharif University of Technology**, July 2014, HOST: Dr. Siavash Bayat
- **Invited Talk: Shahid Beheshti University**, July 2014, HOST: Dr. Ali Jahanian
- **Invited Talk: Amirkabir University of Technology**, June 2014, HOST: Drs. Saheb Zamani and Hamid Zarandi
- **Invited Talk: Cisco Corporation**, May 2014, Host: Dr. Wei Zhao
- **Invited Talk: Xilinx Corporation**, May 2014, Host: Dr. Amit Majumdar
- **Keynote Speaker: IEEE North Atlantic Test Workshop (NATW)**, May 2014
- **Invited Talk: Design, Automation, and Test in Europe (DATE)**, March 2014
- **Keynote Speaker: IEEE Int. Workshop on Reliability-Aware System Design and Test (RASDAT)**, Jan. 2014.
- **Invited Talk: IEEE Microprocessor Test Workshop**, Austin, TX, Dec. 2013
- **Invited Talk: DMSMS**, Dec. 2013, Counterfeit Detect Coverage
- **Invited Talk: DMSMS**, Dec. 2013, Combating Die/IC Recovery
- **Invited Talk: Missile Defense Agency (MDA), PMPB**, Nov. 2013
- **Invited Talk: ARO Workshop**, NYC, Nov. 2013
- **Invited Talk: Honeywell, Cyber Security Group Meeting**, Nov. 2013
- **Invited Talk: National Chao Tung University**, Taiwan, Nov. 2013
- **Invited Talk: MediaTek**, Taiwan, Nov. 2013

- **Invited Talk: CALCE Symposium on Counterfeit Electronic Parts and Electronic Supply Chain**, June 2013
- **Invited Talk: CS1 ICT Supply Chain Risk Management**, June 2013
- **Invited Talk: United Technologies Research Center (UTRC)**, May 2013
- **Invited Talk: NASA Quality Leadership Forum**, March 2013
- **Invited Talk: Trusted Supplier Industry**, March 2013
- **Invited Talk: Cisco, Security Group**, March, 2013, Title: SiliconAP: A novel Platform for Counterfeit Prevention
- **Invited Talk: ARO/CHASE Workshop on Counterfeit Electronics**, Jan. 2013, Counterfeit Detection Assessment
- **Invited Talk: ARO/CHASE Workshop on Counterfeit Electronics**, Jan. 2013, Silicon Authentication Platform
- **Invited Talk: NSF/SRC SA+TS Workshop**, Washington DC, Jan. 2013
- **Invited Talk: Microelectronics Reliability and Qualification proposal (MRQW)**, Dec. 2012
- **Invited Talk: DMSMS Standardization Conference**, Nov. 2012, Title: Secure Split Test for Counterfeit Avoidance
- **Invited Talk: DMSMS Standardization Conference**, Nov. 2012, Title: Counterfeit Test Technology Readiness Assessment
- **Invited Talk: IEEE Asian Test Symposium (ATS)**, Nov. 2012
- **Invited Talk: SRC e-Workshop**, Nov. 2012
- **Invited Talk: University of Arkansas**, Oct. 2012, Host: Prof. Jia Di
- **Invited Talk: Symposium on Counterfeit Electronic Parts and Electronic Supply Chain**, June 2012
- **Invited Talk: University of Pittsburgh**, April 2012, Host: Prof. Kartik Mohanram
- **Invited Talk: University of Illinois at Chicago**, March 2012, Host: Prof. Wenjing Rao
- **Invited Talk: Missile Defense Agency**, March 2012, Host: Fred Schipp
- **Invited Talk: San Jose State University**, March 2012, Host: Prof. Shahab Ardalan
- **Invited Talk: G-19A Test Laboratory Standards Development Committee**, March 2012, Host: Daniel DiMase, Honeywell
- **Invited Talk: IEEE International Reliability Innovations Conference (IRIC)**, March 2012 (Talk on Security)
- **Invited Talk: IEEE International Reliability Innovations Conference (IRIC)**, March 2012 (Talk on Reliability)
- **Invited Talk: IEEE Workshop on Defect and Adaptive Data Analysis (DATA)**, September 2011
- **Invited Talk: Air Force Research laboratory (AFRL)**, Rome, September 2011
- **Invited Talk: University of South Florida**, July 2011, Host: Prof. Sanjukta Bhanja
- **Invited Talk: Low Power SOC Workshop (LPSOC)**, July 2011
- **Invited Talk: IBM TJ Watson**, June 2011, Host: Dr. Peilin Song
- **Invited Talk: Qualcomm**, June 2011, Host: Dr. Sagar Sabade
- **Invited Talk: Cisco**, May 2011, Host: Nemat Bidokhti and Bill Eklow
- **Invited Talk: IEEE VLSI Test Symposium (VTS)**, May 2011, Dana Point, CA
- **Invited Talk: Virginia Tech**, April 22, 2011, Host: Prof. Patrick Schaumont
- **Invited Talk: NYU-Abu Dhabi Workshop on Test**, New York, NY, April 2011, Host: Prof. Ozgur Sinanoglu
- **Invited Talk: University of Maryland**, April 2011, Host: Prof. Gang Qu
- **Invited Talk: ARO Workshop on Hardware Assurance**, Washington, DC, April 2010
- **Invited Talk: University of South Florida**, March 2011, IEEE CS Tampa Chapter, IEEE DVP program
- **Invited Talk: GOMACtech Conference**, March 2011, Orlando, FL

- **Invited Talk: LSI**, March 4, 2011, **Invited by:** Sreejit Chakrabarty, Title: On-chip Measurement Structures: Opportunities and Challenges
- **Invited Talk: LSI**, March 10, 2011, **Invited by:** Arun Gunda, Title: Detection of SDDs in Nanometer Technology Designs
- **Invited Talk: University of Wisconsin, Madison**, Feb. 2011
- **Invited Talk: Freescale**, Austin, TX, Nov. 2010, Host: LeRoy Winemberg
- **Invited Talk: Texas Instruments**, Dallas, TX, September, 2010, Host: Dr. Nisar Ahmed
- **Invited Talk: University of Texas at Arlington**, September 2010, Arlington, TX, HOST: Prof. Robert Magnusson, Title: Design for Hardware Security and Trust
- **Invited Talk: Air Force Research Lab (AFRL)**, Nov. 2011
- **Invited Talk: MediaTek**, Boston, Nov. 2010. Hosts: Jeff Roher and Harry Chen
- **Invited Talk: Cisco**, October 2010, Hosts: Carson Stuart and Nemat Bidokhti, Title: New Threats to Hardware: Detection and Prevention Challenges
- **Invited Talk: Brown University**, Providence, RI, October 2010, Host: Prof. Sherief Reda, Title: Design for Hardware Security and Trust
- **Invited Talk: NYU-Poly**, New York, NY, August 2010, Host: Prof. Ramesh Karri
- **Invited Talk: Qualcomm**, San Diego, CA, August 2010, Host: Mike Laisne
- **Invited Talk: LSI**, June 2010, San Jose, CA, Host: Dr. Sreejit Chakravarty
- **Invited Talk: Cisco**, June 2010, San Jose, CA, Host: Nemat Bidokhti
- **Invited Talk: IBM**, May 2010, Invited by: Dr. Phil Nigh
- **Invited Talk: NASA/ESA Conference on Adaptive Hardware and Systems (AHS-2010)**
- **Invited Talk: Connecticut Microelectronics and Optoelectronics Consortium (CMOC)**, 2010
- **Invited Talk: University of Massachusetts, Lowell**, March 2010, HOST: Prof. Martin Margala
- **Invited Talk: LSI Logic**, Jan 2010, Host: Dr. Sreejit Chakravarty
- **Invited Talk: Information Security Council (INFOSEC)**, Jan 2010
- **Invited Talk: IBM-Austin Research Lab (IBM-ARL)**, Nov. 2009, Host: Dr. Anne Gattiker
- **Invited Talk: ARO Special Workshop** on Hardware Assurance, 2009
- **Invited Talk: AMD**, July 2009, Host: Dr. Mahmut Yilmaz / Jeff Fitzgerald
- **Invited Talk: Amirkabir University of Technology**, July 2009, Host: Dr. A. Bagheri
- **Invited Talk: Cisco**, May 2009, Host: Nemat Bidokhti
- **Invited Talk: Southwest DFT (SWDFT-2009)**, Austin, TX
- **Invited Talk: Duke University**, April 2009, Host: Prof. Krishnendu Chakrabarty
- **Invited Talk: University of Rhode Island**, April 2009, Host: Prof. Resit Sendag
- **Invited Talk: Worcester Polytechnic Institute (WPI)**, March 2009, Host: Prof. Xinming Huang
- **Invited Talk: Mentor Graphics**, Feb 2009, Host: Dr. Yu Huang
- **Invited Talk: IBM TJ Watson**, Nov. 2008, Host: Dr. Jinjun Xiong
- **Invited Talk: Intel**, Nov. 2008, Title: *Small Delay Fault Detection and On-Chip Measurement*
- **Invited Talk: FIST**, Japan, Dec. 2008, Title: *Dealing with Power and Signal Integrity Issues During Test in Nanometer Technology Designs*
- **Invited Talk: University of Connecticut**, Title: *Hardware-Trust: Challenges and Solutions*
- **Invited Talk: IP/IC Trust, University of Connecticut, Northrop Grumman visit**
- **Invited Talk: Fukuoka Industry, Science & Technology Foundation (FIST)**, Japan, Dec. 2008, Title: *Verifying Trustworthiness of Integrated Circuits*
- **Invited Talk: Industry, Science & Technology Foundation (FIST)**, Japan, Dec. 2008, Title: *ATPG for Testing Power Supply Noise and Crosstalk*
- **Invited Talk: IEEE Workshop on Design for Reliability and Variability (DRV)**, Oct. 2008, Title: *ATPG for Increased Quality and In-Field Reliability*

- **Invited Talk: University of Tehran**, Host: Prof. Mahmoud Hashemi, Title: *ATPG for Increased Test Quality and In-field Reliability*
- **Invited Talk: University of Tehran**, Host: Prof. Mahmoud Hashemi, Title: *Verifying the Trustworthiness on Integrated Circuits*
- **Invited Talk: Sharif University of Technology**, Host: Prof. S. Ghassem Miremadi, Title: *ATPG for Increased Test Quality and In-field Reliability*
- **Invited Talk: Babol University of Technology**, Host: Prof. Miar Naimi, Title: *Verifying the Trustworthiness on Integrated Circuits*
- **Invited Talk: IBM**, Aug. 2008, Invited by: Dr. Phil Nigh
- **Invited Talk: Magma**, April 2008, Host: Dr. Sandeep Goel
- **Invited Talk: SRC e-Workshop**, Feb. 2008, **Title:** *High-Quality Delay Tests for Nanotechnology Designs*
- **Invited Talk: Freescale**, Austin, TX, Dec. 2007, Host: Dr. Magdy Abadir/Dr. Raj Raina
- **Invited Talk: Texas Instruments**, Dallas, TX, Dec. 2007, Hosts: Vinay Jayaram / Dr. Ken Butler
- **Invited Talk: TranSwitch**, Bedford, MA, Nov. 2007, Host: Zahi Abuhamdeh
- **Invited Talk: AMD**, Boston, MA, Nov. 2007, Host: Dr. Kamran Zarrineh
- **Invited Talk: Analog Devices**, Boston, MA, Nov. 2007, Host: Harry Chen
- **Keynote Speaker: Magma's Luncheon Event at International Test Conference (ITC)**, San Jose, CA, Tuesday Oct. 23, 2007
- **Invited Talk: Cadence**, June 2007, **Title:** *IR-drop Tolerant At-speed Tests for Nanometer Technology Designs*, Host: Dr. Krishna Chakravadhanula
- **Invited Talk: LSI Logic**, June 2007, **Title:** *Generating High Quality At-speed Tests for Nanometer Technology Designs: Challenges and Solutions*, Invited by: Dr. Sreejit Chakravarty
- **Invited Talk: Qualcomm** (San Diego, CA), June 2007, **Title:** *At-speed Test for Nanotechnology: Challenges and Solutions*, Host: Dr. Sagar Sabade
- **Invited Talk:** Guest Lecturer for VLSI System Testing Course of ECE Department at **Duke University**, Instructor: Prof. Krish Chakrabarty
- **Invited Talk: Mentor Graphics** (Wilsonville, OR), Nov. 2006, **Title:** *At-speed Test for Nanotechnology: Challenges and Solutions*, Host: Dr. Nilanjan Mukherjee
- **Invited Talk: LSI Logic** (San Jose, CA), Nov. 2006, **Title:** *High Quality At-speed Tests for Nanotechnology Designs*, Host: Dr. Arun Gunda
- **Invited Talk: AMD** (Sunnyvale, CA), Oct. 2006, **Title:** *High Quality At-speed Tests for Nanometer High-speed Designs*, Host: Dr. Anuja Sehgal
- **Invited Talk: Texas Instruments** (Dallas, TX), April 2004, **Title:** *Enhanced Scan Architectures for Reducing Power and Test Application Time*

Technology Transfer

1. On-chip Monitors was successfully implemented on few products
2. Small-delay defect generation tool is used by semiconductor and EDA companies
3. LTG Cell for implementing LOS using low-speed scan enable signal
4. SAE International, acquired the CDC tool on counterfeit detection
5. Test point insertion technology for LBIST to semiconductor industry
6. A number of patented technologies are acquired Caspia Technologies, Inc.

Teaching Experience

University of Florida

Fall 2006

ECE 290: Senior Design

Spring 2007

ECE 291: Senior Design

Spring 2007	ECE 300: VLSI Design Verification and Test
Fall 2007	ECE 290: Senior Design
Spring 2008	ECE 291: Senior Design
Spring 2008	ECE 300: VLSI Design Verification and Test
Fall 2008	ECE 4901: Senior Design
Fall 2008	ECE 6094: VLSI CAD Algorithms
Spring 2009	ECE 3421: VLSI Design and Simulation
Fall 2010	ECE 6094: VLSI Design Verification and Test
Fall 2010	ECE 4901: Senior Design
Spring 2010	ECE 4095/6095: Intro. Hardware Security and Trust
Spring 2010	ECE 4902: Senior Design
Fall 2010	ECE 4095/6095: VLSI CAD Algorithms
Fall 2010	ECE 4901: Senior Design
Spring 2011	ECE 3421: VLSI Design and Simulation
Spring 2011	ECE 4902: Senior Design
Fall 2011	ECE 6432: VLSI Design Verification and Testing
Fall 2011	ECE 4901: Senior Design
Fall 2011	ECE 6094: Computer Engineering Seminar
Spring 2012	ECE 3401: Digital Systems Design
Spring 2012	ECE 4902: Senior Design
Spring 2012	ECE 6094: Computer Engineering Seminar
Fall 2012	ECE 4451/5451: Intro. to Hardware Security and Trust
Fall 2012	ECE 4901: Senior Design
Spring 2013	ECE 3401: Digital Systems Design
Spring 2013	ECE 4095: Hardware Hacking
Spring 2013	ECE 4902: Senior Design
Fall 2013	ECE 4901: Senior Design
Spring 2014	ECE 3401: Digital Systems Design
Spring 2014	ECE 4095: Hardware Hacking
Spring 2014	ECE 4902: Senior Design
Fall 2014	ECE 4451/5451: Intro. to Hardware Security and Trust
Fall 2014	ECE 4901: Senior Design
Spring 2015	ECE 4902: Senior Design
Fall 2016	EEL 4714/5716: Intro to Hardware Security and Trust
Fall 2017	EEL 4714/5716: Intro to Hardware Security and Trust
Fall 2018	EEL 4714/5716: Intro to Hardware Security and Trust
Fall 2019	EEL 4714/5716: Intro to Hardware Security and Trust
Fall 2020	EEL 4714/5716: Intro to Hardware Security and Trust
Fall 2021	EEL 4714/5716: Intro to Hardware Security and Trust

New Courses Developed and Taught at UMBC (2004-2006):

SOC Design and Test
CAD Algorithms
VLSI Design Verification and Testing

New Courses Developed and Taught at UConn:

VLSI Design Verification and Testing
CAD Algorithms
Introduction to Hardware Security and Trust
Hardware Hacking

New courses Developed at UF:

Introduction to Hardware Security and Trust

Research Group

Current Post-Doctoral Fellows and Visiting Researchers:

1. **Dr. Sujan Saha**, August 2023 (PhD: University of Florida)
2. **Dr. Jingbo Zhou**, August 2023 (PhD: The Ohio State University)
3. **Dr. Rakibul Hassan**, August 2023 (PhD: George Mason University)

Current Students:

4. **Tanvir Rahman**, PhD Student, Fall 2020, No proposal defense yet, Graduate Sp 26
5. **Shuva Saha**, PhD Student, Spring 2021. Proposal August 6, 25
6. **Azim Uddin**, PhD Student, Spring 2021, Proposal Aug 26, 25
7. **Pantha Sarker**, PhD Student, Spring 2021, Proposal April 25
8. **Ahmed Alhurubi**, PhD Student, Spring 2022
9. **Rasin M. Ihtemam**, PhD Student, Summer 2025
10. **Yasir Mahmut**, PhD Student, Fall 2025

Former Students / Post-doctoral Fellows/Visitors:

Post-doctoral fellow and visiting researchers:

1. **Nitin Varshney**, Lab Engineer, Micron
2. **Dr. Akshay Kulkarni**, Currently with PVAMU
3. **Dr. Kimia Zamiri Azar**, Currently with UCF
4. **Dr. Sree R. Rajendran**, Currently with FAU
5. **Dr. Hadi Mardani**, Currently with UCF
6. **Dr. Fahim Rahman**, CTO, Caspia Technologies
7. **Dr. Nalla Nachimuthu**, Jointly supervised with Prof. Farimah Farahmandi
8. **Dr. Sukanta Dey**, Intel
9. **Daniel Johnson**, Lab Engineer
10. **Dr. Sean Taheri**, Jointly supervised with Prof. Asadi (PhD, University of Central Florida)
11. **Dr. Jungmin Park**, Research Assistant Professor (PhD, Iowa State University), Lucid
12. **Dr. Fahim Rahman**, Research Assistant Professor (PhD, University of Florida)
13. **Dr. Samane Abdi**
14. **Dr. Shahed Quadir**, Currently with Monmouth College
15. **Dr. Rakib Shahriar**, Currently with Cisco
16. **Dr. Shahin Tajik**, Post-doctoral fellow (PhD, TU Berlin), Currently with WPI
17. **Dr. Qihang Shi**, Post-doctoral fellow (PhD, University of Connecticut), Currently with Tsinghua University
18. **Prof. Yun Yang**, Visiting Researcher, Currently with Chang'An University
19. **Dr. Haoting Shen**, Post-doctoral Fellow (PhD, Penn State University), Currently with Zhejiang University
20. **Dr. Xiaolin Xu**, Post-doctoral Fellow, 2016-2018, Currently with Northeastern University
21. **Adam Dundan**, Visiting Researcher, May-August 2018, Navy Crane
22. **Dr. Navid Asadi Zanjani**, Post-doctoral Fellow, 2014-2017, Currently with University of Florida
23. **Dr. Sina Shahbaz**, Post-doctoral Fellow, 2013-2014, Currently with University of Connecticut
24. **Dr. Shuo Wang**, Post-doctoral Fellow, 2010-2012, Currently with Qualcomm
25. **Dr. Hassan Salmani**, Post-doctoral Fellow, 2011-2013, Currently with Howard University

Graduated PhD Students:

1. **Nisar Ahmed**, PhD, Oct. 2007, Currently with Apple
2. **Junxia Ma**, Dec. 2010, Currently with Intel
3. **Ke Peng**, Dec. 2010, Currently with ARM
4. **Xiaoxiao (Michel) Wang**, Dec. 2010, Currently with Beihang University

5. **Jeremy Lee**, Dec. 2010, Currently with Texas Instruments
6. **Hassan Salmani**, August 2011, Howard University
7. **Wei Zhao**, 2013, Currently with Nvidia
8. **Xuehui Zhang**, 2013, Currently with Oracle
9. **Jifeng Chen**, 2013, Currently with Samsung Research America
10. **Fang Bao**, 2014, Currently with Intel
11. **Kan Xiao**, 2015, Currently with Intel
12. **Ujjwal Guin**, 2016, Currently an Assistant Professor at Auburn University
13. **Mehdi Sadi**, 2017, Currently with Auburn University
14. **Gustavo Contreras**, 2017, Currently with Intel
15. **Qihang Shi**, 2017, Currently a post-doc at the University of Florida
16. **Tauhidur Rahman**, 2017, Currently with the University of Alabama
17. **Kun Yang**, Jan 2018, Professpr at Zhejiang University
18. **Fahim Rahman**, July 2018, CTO, Caspia Technologies
19. **Tony (Miao) He**, July 2018
20. **Adib Nahiyani**, Aug 2019, Currently with Intel
21. **Huanyu Wang**, April 2021, Currently with Apple
22. **Jason Vosatka**, April 2021, Scientist, AFB Eglin
23. **Andrew Stern**, August 2021, CEO, Coremeleon
24. **Dhwani Mehta**, July 2022, Currently with AMD
25. **Nidish Vashistha**, July 2022, Currently with Micron
26. **Nitin Pundir**, July 2022, Currently with IBM
27. **Mohammad Farmani**, July 2022
28. **Sazadur Rahman**, Dec. 2022, Intel, then joined University of Central Florida
29. **Nusrat Farzana**, Navidia, Dec. 2023, Currently with NVIDIA
30. **Jacob Harrison**, Bloomberg, Aug 2023, Currently with Bloomberg
31. **Monir Rahman**, August 2024, Joined AMD
32. **Bulbul Ahmed**, August 2024, Joined NVIDIA
33. **Md. Sami Ul Islam**, Fall 2024, Joined NVIDIA
34. **Henian Li**, Spring 2025, Joined Qualcomm
35. **Amit Mazumder**, Summer 2025
36. **Hasan Al-Shaikh**, Summer 2025
37. **Kawser Bepary**, Summer 2025
38. **Nurun Mondol**, Summer 2025
39. **Paul Calzada**, Summer 2025
40. **Rasheed Kibira**, Fall 2025
41. **Md Latifur Rahman**, Fall 2025
42. **Md Saad Haque**, Fall 2025
43. **Mohammad Monjil**, Fall 2025
44. **Shang Shi**, Fall 2025

Graduated M.Sc. Students:

1. **Hector Crespo**, May 2022
2. **Ashley Tramble**, May 2021
3. **Halit Dogan**, Sep. 2013, Currently with University of Connecticut
4. **Niranjan Kayam**, M.S., Sep. 2011, Currently with Synopsys
5. **Prasath Periyasamy**, M.S. Thesis, Aug 2006, Currently with Qualcomm
6. **Smita Patil**, M.S. Project, Aug 2006, Currently with Atmel
7. **Mohammed ElShoukry**, M.S. Thesis, Aug 2006, Currently with Micron
8. **Eun Chung**, M.S. Project, Dec. 2004

Undergraduate Students:

1. Brandon Wand, Undergraduate, Summer 2020
2. Luran Manfino, Undergraduate, Summer 2020
3. Anna Raymaker, Undergraduate, May 2020-Jan 2022
4. Paul Calzada, Undergraduate, Fall 2019-Spring & Summer 2020
5. Risham Sidhu, 2018
6. Wesley Steven, 2014
7. Dan Guerrero, 2014
8. Ryan Nesbit, 2014
9. Shane Tobey, 2013
10. Shane Kelly, 2013-2014
11. Nathan Murphy, 2013
12. Jacquelyn Khajah, 2014
13. Andrew Ferraiuolo, REU-Sponsored Undergraduate Student, Summer & Fall 2011, Spring 2012
14. Ashley Calder, Undergraduate Student, Spring 2012
15. Michael Calvo, Eastern Conn. Univ., REU-Sponsored Undergraduate Student, Summer 2011
16. Sagar Patil, Undergraduate Researcher, Summer 2010
17. Ryan Fitterman (CMPE), Senior Design, 2012
18. Jeffrey Foster (EE), Senior Design, 2012
19. Alvin Sanabria (EE), Senior Design, 2012
20. Michael Stettenbenz (EE), Senior Design, 2012
21. Rifat Chowdhury (CMPE/MATH), Senior Design, 2012
22. Andrew Ferraiuolo (EE/CMPE), Senior Design, 2012
23. Adam Zimmer (CSE), Senior Design, 2012
24. Carl Hinkle (EE), Senior Design, 2011
25. Dan Matosian (CMPE), Senior Design, 2011
26. Ryan Wilson (EE), Senior Design, 2011
27. Emilio Cepeda (EE), Senior Design, 2011
28. Theodore Estwan (EE), Senior Design, 2011
29. Brian Helfer (EE), Senior Design, 2011
30. Sagar Patel (EE), Senior Design, 2010
31. Michael Runde (CMPE), Senior Design, 2010
32. Ton Thomas (CMPE), Senior Design, 2010
33. Nicholas Tuzzio (CMPE), Senior Design, 2010
34. Corey Benoit (EE), Senior Design, 2010
35. Joesph Larosa (EE), Senior Design, 2010
36. Kevin Perkins (EE), Senior Design, 2010
37. Andrew Tan (EE/MGMT), Senior Design, 2009
38. Colin Gladding (EE), Senior Design, 2009
39. Harpreet Mankoo (EE), Senior Design, 2009
40. Joe Mascola (EE), Senior Design, 2009
41. Elvis Anes (CMPE), Senior Design, 2009
42. Jeff Chua (CMPE), Senior Design, 2009
43. Ali Faraz (EE), Senior Design, 2009
44. Samantha Logue (CMPE), Senior Design, 2009
45. Poorak Mody (CMPE), Senior Design, 2008
46. Jonathan Schindler (CMPE), Senior Design, 2008
47. Jason Thibodeau (CMPE), Senior Design, 2008
48. Aaron Feldstein (EE), Senior Design, 2008
49. Paul Rago (EE), Senior Design, 2008
50. Danny Ho (EE), Senior Design, 2007

51. Kevin Tyler (EE), Senior Design, 2007
52. Vimal Vacchani (EE), Senior Design, 2007
53. Michael Kelley (EE), Senior Design, 2007
54. Benjamin Romeo (EE), Senior Design, 2007
55. Jeffrey Travis (EE), Senior Design, 2007
56. Pedro Almada, B.S., 2005

Thesis Advisory Committee

PhD Advisory Committee:

Nisar Ahmed (Chair), Jianwei Dai (Advisor: Lei Wang, UConn), Wei-Gu Tang (Advisor: Lei Wang, UConn), Janardhan Singaraju (Advisor: John Chandy, UConn), Junxia Ma (Chair), Ke Peng (Chair), Michel Wang (Chair), Xuan Guan (Advisor: Yungsi Fei), Jeremy Lee (Chair), Hai Lin, Shou Wang, Tina John (Advisor: John Chandy, UConn), Abhishek Singh (Advisor: Jim Plusquellic, UMB), Ajith Kumar (Advisor: John Chandy, UConn), Robert Karam (Advisor: Swarup Bhunia, UF, 2017), Zimu Guo (Advisor: Domenic Forte, UF), Gustavo Contreras (Chair), Tauhid Rahman (Chair), Mahmut Yilmaz (Advisor: Krishnendu Chakrabarty, Duke University); Nolen Scaife (Advisor: Patrick Traynor, UF, 2018), Kai Yang (Advisor: Swarup Bhunia, UF, 2018), Fangchao Zhang (Advisor: Swarup Bhunia, UF, 2018), Nima Karimian (Advisor: Domenic Forte, UConn, 2018), Zimu Guo (Advisor: Domenic Forte, UF), Abdulrahman Alql (Advisor: Swarup Bhunia), Mukhil Azhagan (Advisor: Navid Asadi), Alice Hangwei (Advisor: Damon Woodard), Ana Covic (Advisor: Domenic Forte), Tamzidul Hoque (Advisor: Swarup Bhunia), Christian Peeters (Advisor: Patrick Traynor), Alice Lu (Advisor: Damon Woodard), Rabin Acharya (Advisor: Domenic Forte)

International: Fatemeh Ganji (Advisor: Jean-Pierre Seifert, TU Berlin, 2018), Shahin Tajik (Advisor: Jean-Pierre Seifert, TU Berlin, 2018)

M.S. Advisory Committee:

Halit Dogan (Chair), Niranjana Kayam (Chair), Prasath Periyasamy (Chair), Smita Patil (Chair), Mohammed ElShoukry (Chair), Eun Chung (Chair), Pushkar Pulastya, Michael Wolk, Jitin Tharian, Adhruva Acharyya, Niranjana Reddy, Shruti Khare, Michael Runda, Hitesh Sharma

B.Sc. Advisory Committee:

Jackson Carrol

Institutional Service

- UF: ECE/CISE Department Chair, Wally Rhines Chair Professorship in Homomorphic Professorships (2021)
- UF: ECE Department, Chair, Semotto IoT Chair Professorship Search Committee (2018-2019)
- UF: College of Engineering, Tenure & Promotion (T&P) Committee (2017-2019)
- UF: ECE Department, Chair, Tenure & Promotion (T&P) Committee (2017-2019)
- UF: ECE Department, Associate Chair for Research and Strategic Initiatives (2017-present)
- UF: College of Engineering, Member, Research Advancement Committee, RAC (2017-present)
- UF: ECE Department, Chair, Faculty Development Committee (2017-present)
- UF: ECE Department, Member, Semotto IoT Chair Professorship Search Committee (2017-2018)
- UF: College of Engineering, Tenure & Promotion (T&P) Committee (2017-2020)
- UConn: Chair, Computer Engineering Search Committee (2012-2014)
- UConn: ECE Search Committee (2011-2012, 2013-2014)
- UConn: ECE Department Library Liaison, January 2009-Present
- UConn: C&C Committee (2007-present)

- UMBC: Member, Equipment Committee (Oct. 2004–2006)
- UMBC: Member, Graduate Admission Committee (Jan 2005-2006)
- UMBC: Member, ABET Visiting Committee (Oct. 2004–2006)

Supervising Undergraduate Senior Design Projects

2006-2007	Project 1: Redesign of Solitec Track System (Sponsored by Phonon) Project 2: Speech Control System for Persons with Disabilities (Sponsored by ECE Department) First Prize in ECE Department
2007-2008	Project 1: Wafer Processing Track Upgrade (Sponsored by Phonon) Second Prize in ECE Department Project 2: CAD2XML (Sponsored by QualTech)
2008-2009	Project 1: Digital Temperature Controller (DTC) Design (Sponsored by Phonon) Project 2: UConn Personal ATE (Sponsored by ECE Department)
2009-2010	Project 1: Surface Contour Profiler (Sponsored by Phonon) First Prize in ECE Department Project 2: UConn Personal ATE (Sponsored by ECE Department)
2010-2011	Project 1: Enhanced Surface Contour Profiler (Sponsored by Phonon) First Prize in ECE Department Project 2: Distributed Aviation Control and Communication System (Sponsored by Hamilton Sundstrand)
2011-2012	Project 1: Automated Trojan Insertion and Detection Evaluation (Sponsored by ECE Department) First Prize in ECE Department Project 2: Distributed Aviation Control and Communication System (Sponsored by Hamilton Sundstrand)
2013-2014	Project 1: Virtual Laboratory for Hardware Security (Sponsored by ECE Department) Project 2: Automated Counterfeit IC Physical Defect Characterization (Sponsored by ECE Department)